AM243x Sitara™ Microcontrollers

1 Features

Processor cores:

- Up to 2× Dual-core Arm Cortex®-R5F MCU subsystems operating at up to 800 MHz, highly-integrated for real-time processing
  - Dual-core Arm Cortex®-R5F clusters support dual-core and single-core operation
  - 32KB ICache and 32KB DCache per R5F core with SECDED ECC on all memories
  - Single-core: 128KB TCM per cluster (128KB TCM per R5F core)
  - Dual-core: 128KB TCM per cluster (64KB TCM per R5F core)
- 1× Single-core Arm Cortex®-M4F MCU at up to 400 MHz
  - 256KB SRAM with SECDED ECC

Memory subsystem:

- Up to 2MB of On-chip RAM (OCSRAM) with SECDED ECC:
  - Can be divided into smaller banks in increments of 256KB for as many as 8 separate memory banks
  - Each memory bank can be allocated to a single core to facilitate software task partitioning
- DDR Subsystem (DDRSS)
  - Supports LPDDR4, DDR4 memory types
  - 16-Bit data bus with inline ECC
  - Supports speeds up to 1600 MT/s

System on Chip (SoC) services:

- Device Management Security Controller (DMSC-L)
  - Centralized SoC system controller
  - Manages system services including initial boot, security, and clock/reset/power management
  - Communication with various processing units over message manager
  - Simplified interface for optimizing unused peripherals
  - On-Chip Debug functionality through JTAG and Trace interfaces)
- Data Movement Subsystem (DMSS)
  - Block Copy DMA (BCDMA)
  - Packet DMA (PKTDMA)
  - Secure Proxy (SEC_PROXY)
  - Ring Accelerator (RINGACC)
- Time Sync Subsystem
  - Central Platform Time Sync (CPTS) module
  - Timer Manager (TIMERMANAGER) with 1024 timers
  - Time Sync and Compare event interrupt routers

Industrial subsystem:

- 2× Gigabit Industrial Communication Subsystems (PRU_ICSSG)
  - Optional support for Profinet IRT, Profinet RT, EtherNet/IP, EtherCAT, Time-Sensitive Networking (TSN), and other Networking Protocols
  - Backwards compatibility with 10/100Mb PRU_ICSS
  - Each PRU_ICSSG contains:
    - 3× PRU RISC Cores per Slice (2× Slice per PRU_ICSSG)
      - PRU General Use core (PRU)
      - PRU Real-Time Unit core (PRU-RTU)
      - PRU Transmit core (PRU-TX)
    - Each PRU core supports the following features:
      - Instruction RAM with ECC
      - Broadside RAM
      - Multiplier with optional accumulator (MAC)
      - CRC16/32 hardware accelerator
      - Byte swap for Big/Little Endian conversion
      - SUM32 hardware accelerator for UDP checksum
      - Task Manager for preemption support
    - Up to 2× Ethernet ports
      - RGMII (10/100/1000)
      - MII (10/100)
    - Three Data RAMs with ECC
    - 8 banks of 30 × 32-bit register scratchpad memory
    - Interrupt controller and task manager
    - 2× 64-bit Industrial Ethernet Peripherals (IEPs) for time stamping and other time synchronization functions
    - 18× Sigma-Delta Filter Module (SDFM) interfaces
      - Short circuit logic
      - Over-current logic
    - 6× Multi-protocol position encoder interfaces
    - 1× Enhanced Capture Module (ECAP)
    - 16550-compatible UART
      - Dedicated 192-MHz clock to support 12-Mbps PROFIBUS

Security:

- Secure Boot supported
  - Hardware-enforced Root-of-Trust (RoT)
  - Support to switch RoT via backup key
  - Support for takeover protection, IP protection, and anti-roll back protection
- Support for cryptographic acceleration
  - Session-aware cryptographic engine with ability to auto-switch key-material based on incoming data stream
  - DMA support
  - Supports cryptographic cores
    - AES – 128/192/256-bit key sizes
    - 3DES – 56/112/168-bit key sizes
    - MD5, SHA1
    - SHA2 – 224/256/384/512-bit key sizes
    - DRBG with true random number generator
    - PKA (Public Key Accelerator) to Assist in RSA/ECC processing
- Debugging security
  - Secure software-controlled debug access
  - Security aware debugging
- Secure storage support
- On-the-Fly encryption (OTFE) support for OSPI in XIP mode
- Networking security support for data (Payload) encryption/authentication via packet-based hardware cryptographic engine
- DMSC-L co-processor for security and key management, with dedicated device level interconnect

General connectivity peripherals:

- 6× Inter-Integrated Circuit (I2C) ports
- 9× configurable Universal Asynchronous Receive/ Transmit (UART) modules
- 1× 12-bit Analog-to-Digital Converters (ADC)
  - Configurable sample rate up to 4 MSPS
  - 8× multiplexed analog inputs
- 7× Multichannel Serial Peripheral Interfaces (SPI) controllers
- 3× General-Purpose I/O (GPIO) modules

Industrial and control interfaces:

- 9× Enhanced Pulse-Width Modulator (EPWM) modules
- 3× Enhanced Capture (ECAP) modules
- 3× Enhanced Quadrature Encoder Pulse (EQEP) modules
- 2× Modular Controller Area Network (MCAN) modules with full CAN-FD support
- 2× Fast Serial Interface Transmitter (FSITX) cores
- 6× Fast Serial Interface Receiver (FSIRX) cores

High-speed interfaces:

- 1× Integrated Ethernet switch supporting up to 2 external ports (CPSW3G)
  - Up to 2 Ethernet ports
    - RGMII (10/100/1000)
    - RMII (10/100)
  - IEEE 1588 (2008 Annex D, Annex E, Annex F) with 802.1AS PTP
  - Clause 45 MDIO PHY management
  - Energy efficient Ethernet (802.3az)
- 1× PCI-Express® Gen2 controller (PCIE)
  - Supports Gen2 Single Lane operation
- 1× USB 3.1 Dual-Role Device (DRD) Subsystem (USBSS)
  - Port configurable as USB host, USB device, or USB Dual-Role device
  - USB device: High-speed (480 Mbps) and Full-speed (12 Mbps)
  - USB host: SuperSpeed Gen 1 (5 Gbps), High-speed (480 Mbps),Full-speed (12 Mbps), and Low-speed (1.5 Mbps)
  - Integrated USB VBUS detection
- 1× Serializer/Deserializer (SERDES)
  - One SerDes PHY lane to support either PCI-Express® Gen2 or USB Super-Speed Gen1

Media and data storage:

- 2× MultiMedia Card/Secure Digital (MMCSD) interfaces
  - One 8-bit for eMMC (MMCSD0)
  - One 4-bit for SD/SDIO (MMCSD1)
  - Integrated analog switch for voltage switching between 3.3V to 1.8V for high-speed cards
- 1× General-Purpose Memory Controller (GPMC)
  - 16-bit parallel bus with 133 MHz clock or
  - 32-bit parallel bus with 100 MHz clock
  - Error Location Module (ELM) support
- 1× Flash Subsystem (FSS) that can be configured as one Octal SPI (OSPI) or one Quad SPI (QSPI) flash interface

Power management:

- Simplified power sequencing requirements
- Dual-voltage I/O Support
- Integrated SDIO LDO for handling automatic voltage transition for SD interface
- Integrated voltage supervisor for safety monitoring of over-under voltage conditions
- Integrated power supply glitch detector for detecting fast supply transients