Table 8-6. GPIO Configuration for High-Speed SPI (continued)

GPIO	SPI Signal	Mux Configuration	
GPIO61	SPISTEA	GPBGMUX2[27:26]=11	GPBMUX2[27:26]=11
GPIO63	SPISIMOB	GPBGMUX2[31:30]=11	GPBMUX2[31:30]=11
GPIO64	SPISOMIB	GPCGMUX1[1:0]=11	GPCMUX1[1:0]=11
GPIO65	SPICLKB	GPCGMUX1[3:2]=11	GPCMUX1[3:2]=11
GPIO66	SPISTEB	GPCGMUX1[5:4]=11	GPCMUX1[5:4]=11
GPIO69	SPISIMOC	GPCGMUX1[11:10]=11	GPCMUX1[11:10]=11
GPIO70	SPISOMIC	GPCGMUX1[13:12]=11	GPCMUX1[13:12]=11
GPIO71	SPICLKC	GPCGMUX1[15:14]=11	GPCMUX1[15:14]=11
GPIO72	SPISTEC	GPCGMUX1[17:16]=11	GPCMUX1[17:16]=11

8.7 GPIO and Peripheral Muxing

Up to twelve different peripheral functions are multiplexed to each pin along with a general-purpose input/output (GPIO) function. This allows you to choose the peripheral mix and pinout that will work best for your particular application. Refer to the table below for muxing combinations and definitions.

Table 8-7. GPIO Muxed Pins(1)(2)

	GPIO Mux Selection							
GPIO Index	**0, 4, 8, 12**	**1**	**2**	**3**	**5**	**6**	**7**	**15**
GPyGMUXn. GPIOz =	**00b, 01b, 10b, 11b**	**00b**			**01b**			**11b**
GPyMUXn. GPIOz =	**00b**	**01b**	**10b**	**11b**	**01b**	**10b**	**11b**	**11b**
	GPIO0	EPWM1A (O)				SDAA (I/OD)		
	GPIO1	EPWM1B (O)		MFSRB (I/O)		SCLA (I/OD)		
	GPIO2	EPWM2A (O)			OUTPUTXBAR1 (O)	SDAB (I/OD)		
	GPIO3	EPWM2B (O)	OUTPUTXBAR2 (O)	MCLKRB (I/O)	OUTPUTXBAR2 (O)	SCLB (I/OD)		
	GPIO4	EPWM3A (O)			OUTPUTXBAR3 (O)	CANTXA (O)		
	GPIO5	EPWM3B (O)	MFSRA (I/O)	OUTPUTXBAR3 (O)		CANRXA (I)		
	GPIO6	EPWM4A (O)	OUTPUTXBAR4 (O)	EXTSYNCOUT (O)	EQEP3A (I)	CANTXB (O)		
	GPIO7	EPWM4B (O)	MCLKRA (I/O)	OUTPUTXBAR5 (O)	EQEP3B (I)	CANRXB (I)		
	GPIO8	EPWM5A (O)	CANTXB (O)	ADCSOCAO (O)	EQEP3S (I/O)	SCITXDA (O)		
	GPIO9	EPWM5B (O)	SCITXDB (O)	OUTPUTXBAR6 (O)	EQEP3I (I/O)	SCIRXDA (I)		
	GPIO10	EPWM6A (O)	CANRXB (I)	ADCSOCBO (O)	EQEP1A (I)	SCITXDB (O)		UPP-WAIT (I/O)
	GPIO11	EPWM6B (O)	SCIRXDB (I)	OUTPUTXBAR7 (O)	EQEP1B (I)	SCIRXDB (I)		UPP-START (I/O)
	GPIO12	EPWM7A (O)	CANTXB (O)	MDXB (O)	EQEP1S (I/O)	SCITXDC (O)		UPP-ENA (I/O)
	GPIO13	EPWM7B (O)	CANRXB (I)	MDRB (I)	EQEP1I (I/O)	SCIRXDC (I)		UPP-D7 (I/O)
	GPIO14	EPWM8A (O)	SCITXDB (O)	MCLKXB (I/O)		OUTPUTXBAR3 (O)		UPP-D6 (I/O)
	GPIO15	EPWM8B (O)	SCIRXDB (I)	MFSXB (I/O)		OUTPUTXBAR4 (O)		UPP-D5 (I/O)
	GPIO16	SPISIMOA (I/O)	CANTXB (O)	OUTPUTXBAR7 (O)	EPWM9A (O)		SD1_D1 (I)	UPP-D4 (I/O)
	GPIO17	SPISOMIA (I/O)	CANRXB (I)	OUTPUTXBAR8 (O)	EPWM9B (O)		SD1_C1 (I)	UPP-D3 (I/O)
	GPIO18	SPICLKA (I/O)	SCITXDB (O)	CANRXA (I)	EPWM10A (O)		SD1_D2 (I)	UPP-D2 (I/O)
	GPIO19	SPISTEA (I/O)	SCIRXDB (I)	CANTXA (O)	EPWM10B (O)		SD1_C2 (I)	UPP-D1 (I/O)
	GPIO20	EQEP1A (I)	MDXA (O)	CANTXB (O)	EPWM11A (O)		SD1_D3 (I)	UPP-D0 (I/O)

(1) I = Input, O = Output, OD = Open Drain

(2) GPIO Index settings of 9, 10, 11, 13, and 14 are reserved.

Table 8-7. GPIO Muxed Pins[1][2] (continued)

	GPIO Mux Selection							
GPIO Index	**0, 4, 8, 12**	**1**	**2**	**3**	**5**	**6**	**7**	**15**
GPyGMUXn. GPIOz =	**00b, 01b, 10b, 11b**	**00b**			**01b**			**11b**
GPyMUXn. GPIOz =	**00b**	**01b**	**10b**	**11b**	**01b**	**10b**	**11b**	**11b**
	GPIO21	EQEP1B (I)	MDRA (I)	CANRXB (I)	EPWM11B (O)		SD1_C3 (I)	UPP-CLK (I/O)
	GPIO22	EQEP1S (I/O)	MCLKXA (I/O)	SCITXDB (O)	EPWM12A (O)	SPICLKB (I/O)	SD1_D4 (I)	
	GPIO23	EQEP1I (I/O)	MFSXA (I/O)	SCIRXDB (I)	EPWM12B (O)	SPISTEB (I/O)	SD1_C4 (I)	
	GPIO24	OUTPUTXBAR1 (O)	EQEP2A (I)	MDXB (O)		SPISIMOB (I/O)	SD2_D1 (I)	
	GPIO25	OUTPUTXBAR2 (O)	EQEP2B (I)	MDRB (I)		SPISOMIB (I/O)	SD2_C1 (I)	
	GPIO26	OUTPUTXBAR3 (O)	EQEP2I (I/O)	MCLKXB (I/O)	OUTPUTXBAR3 (O)	SPICLKB (I/O)	SD2_D2 (I)	
	GPIO27	OUTPUTXBAR4 (O)	EQEP2S (I/O)	MFSXB (I/O)	OUTPUTXBAR4 (O)	SPISTEB (I/O)	SD2_C2 (I)	
	GPIO28	SCIRXDA (I)	EM1CS4 (O)		OUTPUTXBAR5 (O)	EQEP3A (I)	SD2_D3 (I)	
	GPIO29	SCITXDA (O)	EM1SDCKE (O)		OUTPUTXBAR6 (O)	EQEP3B (I)	SD2_C3 (I)	
	GPIO30	CANRXA (I)	EM1CLK (O)		OUTPUTXBAR7 (O)	EQEP3S (I/O)	SD2_D4 (I)	
	GPIO31	CANTXA (O)	EM1WE (O)		OUTPUTXBAR8 (O)	EQEP3I (I/O)	SD2_C4 (I)	
	GPIO32	SDAA (I/OD)	EM1CS0 (O)					
	GPIO33	SCLA (I/OD)	EM1RNW (O)					
	GPIO34	OUTPUTXBAR1 (O)	EM1CS2 (O)			SDAB (I/OD)		
	GPIO35	SCIRXDA (I)	EM1CS3 (O)			SCLB (I/OD)		
	GPIO36	SCITXDA (O)	EM1WAIT (I)			CANRXA (I)		
	GPIO37	OUTPUTXBAR2 (O)	EM1OE (O)			CANTXA (O)		
	GPIO38		EM1A0 (O)		SCITXDC (O)	CANTXB (O)		
	GPIO39		EM1A1 (O)		SCIRXDC (I)	CANRXB (I)		
	GPIO40		EM1A2 (O)			SDAB (I/OD)		
	GPIO41		EM1A3 (O)			SCLB (I/OD)		
	GPIO42					SDAA (I/OD)		SCITXDA (O)
	GPIO43					SCLA (I/OD)		SCIRXDA (I)
	GPIO44		EM1A4 (O)					
	GPIO45		EM1A5 (O)					
	GPIO46		EM1A6 (O)			SCIRXDD (I)		
	GPIO47		EM1A7 (O)			SCITXDD (O)		
	GPIO48	OUTPUTXBAR3 (O)	EM1A8 (O)			SCITXDA (O)	SD1_D1 (I)	
	GPIO49	OUTPUTXBAR4 (O)	EM1A9 (O)			SCIRXDA (I)	SD1_C1 (I)	
	GPIO50	EQEP1A (I)	EM1A10 (O)			SPISIMOC (I/O)	SD1_D2 (I)	
	GPIO51	EQEP1B (I)	EM1A11 (O)			SPISOMIC (I/O)	SD1_C2 (I)	
	GPIO52	EQEP1S (I/O)	EM1A12 (O)			SPICLKC (I/O)	SD1_D3 (I)	
	GPIO53	EQEP1I (I/O)	EM1D31 (I/O)	EM2D15 (I/O)		SPISTEC (I/O)	SD1_C3 (I)	
	GPIO54	SPISIMOA (I/O)	EM1D30 (I/O)	EM2D14 (I/O)	EQEP2A (I)	SCITXDB (O)	SD1_D4 (I)	
	GPIO55	SPISOMIA (I/O)	EM1D29 (I/O)	EM2D13 (I/O)	EQEP2B (I)	SCIRXDB (I)	SD1_C4 (I)	
	GPIO56	SPICLKA (I/O)	EM1D28 (I/O)	EM2D12 (I/O)	EQEP2S (I/O)	SCITXDC (O)	SD2_D1 (I)	
	GPIO57	SPISTEA (I/O)	EM1D27 (I/O)	EM2D11 (I/O)	EQEP2I (I/O)	SCIRXDC (I)	SD2_C1 (I)	
	GPIO58	MCLKRA (I/O)	EM1D26 (I/O)	EM2D10 (I/O)	OUTPUTXBAR1 (O)	SPICLKB (I/O)	SD2_D2 (I)	SPISIMOA[3] (I/O)
	GPIO59	MFSRA (I/O)	EM1D25 (I/O)	EM2D9 (I/O)	OUTPUTXBAR2 (O)	SPISTEB (I/O)	SD2_C2 (I)	SPISOMIA[3] (I/O)
	GPIO60	MCLKRB (I/O)	EM1D24 (I/O)	EM2D8 (I/O)	OUTPUTXBAR3 (O)	SPISIMOB (I/O)	SD2_D3 (I)	SPICLKA[3] (I/O)

(3) High-Speed SPI-enabled GPIO mux option. This pin mux option is required when using the SPI in High-Speed Mode (HS_MODE = 1 in SPICCR). This mux option is still available when not using the SPI in High-Speed Mode (HS_MODE = 0 in SPICCR).

Table 8-7. GPIO Muxed Pins[1][2] (continued)

	GPIO Mux Selection							
GPIO Index	**0, 4, 8, 12**	**1**	**2**	**3**	**5**	**6**	**7**	**15**
GPyGMUXn. GPIOz =	**00b, 01b, 10b, 11b**	**00b**			**01b**			**11b**
GPyMUXn. GPIOz =	**00b**	**01b**	**10b**	**11b**	**01b**	**10b**	**11b**	**11b**
	GPIO61	MFSRB (I/O)	EM1D23 (I/O)	EM2D7 (I/O)	OUTPUTXBAR4 (O)	SPISOMIB (I/O)	SD2_C3 (I)	$\overline{\text{SPISTEA}}$[3] (I/O)
	GPIO62	SCIRXDC (I)	EM1D22 (I/O)	EM2D6 (I/O)	EQEP3A (I)	CANRXA (I)	SD2_D4 (I)	
	GPIO63	SCITXDC (O)	EM1D21 (I/O)	EM2D5 (I/O)	EQEP3B (I)	CANTXA (O)	SD2_C4 (I)	SPISIMOB[3] (I/O)
	GPIO64		EM1D20 (I/O)	EM2D4 (I/O)	EQEP3S (I/O)	SCIRXDA (I)		SPISOMIB[3] (I/O)
	GPIO65		EM1D19 (I/O)	EM2D3 (I/O)	EQEP3I (I/O)	SCITXDA (O)		SPICLKB[3] (I/O)
	GPIO66		EM1D18 (I/O)	EM2D2 (I/O)		SDAB (I/OD)		$\overline{\text{SPISTEB}}$[3] (I/O)
	GPIO67		EM1D17 (I/O)	EM2D1 (I/O)				
	GPIO68		EM1D16 (I/O)	EM2D0 (I/O)				
	GPIO69		EM1D15 (I/O)			SCLB (I/OD)		SPISIMOC[3] (I/O)
	GPIO70		EM1D14 (I/O)		CANRXA (I)	SCITXDB (O)		SPISOMIC[3] (I/O)
	GPIO71		EM1D13 (I/O)		CANTXA (O)	SCIRXDB (I)		SPICLKC[3] (I/O)
	GPIO72		EM1D12 (I/O)		CANTXB (O)	SCITXDC (O)		$\overline{\text{SPISTEC}}$[3] (I/O)
	GPIO73		EM1D11 (I/O)	XCLKOUT (O)	CANRXB (I)	SCIRXDC (I)		
	GPIO74		EM1D10 (I/O)					
	GPIO75		EM1D9 (I/O)					
	GPIO76		EM1D8 (I/O)			SCITXDD (O)		
	GPIO77		EM1D7 (I/O)			SCIRXDD (I)		
	GPIO78		EM1D6 (I/O)			EQEP2A (I)		
	GPIO79		EM1D5 (I/O)			EQEP2B (I)		
	GPIO80		EM1D4 (I/O)			EQEP2S (I/O)		
	GPIO81		EM1D3 (I/O)			EQEP2I (I/O)		
	GPIO82		EM1D2 (I/O)					
	GPIO83		EM1D1 (I/O)					
	GPIO84				SCITXDA (O)	MDXB (O)		MDXA (O)
	GPIO85		EM1D0 (I/O)		SCIRXDA (I)	MDRB (I)		MDRA (I)
	GPIO86		EM1A13 (O)	EM1CAS (O)	SCITXDB (O)	MCLKXB (I/O)		MCLKXA (I/O)
	GPIO87		EM1A14 (O)	EM1RAS (O)	SCIRXDB (I)	MFSXB (I/O)		MFSXA (I/O)
	GPIO88		EM1A15 (O)	EM1DQM0 (O)				
	GPIO89		EM1A16 (O)	EM1DQM1 (O)		SCITXDC (O)		
	GPIO90		EM1A17 (O)	EM1DQM2 (O)		SCIRXDC (I)		
	GPIO91		EM1A18 (O)	EM1DQM3 (O)		SDAA (I/OD)		
	GPIO92		EM1A19 (O)	EM1BA1 (O)		SCLA (I/OD)		
	GPIO93			EM1BA0 (O)		SCITXDD (O)		
	GPIO94					SCIRXDD (I)		
	GPIO95							
	GPIO96			EM2DQM1 (O)	EQEP1A (I)			
	GPIO97			EM2DQM0 (O)	EQEP1B (I)			
	GPIO98			EM2A0 (O)	EQEP1S (I/O)			
	GPIO99			EM2A1 (O)	EQEP1I (I/O)			
	GPIO100			EM2A2 (O)	EQEP2A (I)	SPISIMOC (I/O)		
	GPIO101			EM2A3 (O)	EQEP2B (I)	SPISOMIC (I/O)		
	GPIO102			EM2A4 (O)	EQEP2S (I/O)	SPICLKC (I/O)		
	GPIO103			EM2A5 (O)	EQEP2I (I/O)	$\overline{\text{SPISTEC}}$ (I/O)		
	GPIO104	SDAA (I/OD)		EM2A6 (O)	EQEP3A (I)	SCITXDD (O)		
	GPIO105	SCLA (I/OD)		EM2A7 (O)	EQEP3B (I)	SCIRXDD (I)		
	GPIO106			EM2A8 (O)	EQEP3S (I/O)	SCITXDC (O)		
	GPIO107			EM2A9 (O)	EQEP3I (I/O)	SCIRXDC (I)		
	GPIO108			EM2A10 (O)				
	GPIO109			EM2A11 (O)				
	GPIO110			EM2WAIT (I)				
	GPIO111			EM2BA0 (O)				

Table 8-7. GPIO Muxed Pins[1][2] (continued)

	GPIO Mux Selection							
GPIO Index	**0, 4, 8, 12**	**1**	**2**	**3**	**5**	**6**	**7**	**15**
GPyGMUXn. GPIOz =	**00b, 01b, 10b, 11b**	**00b**			**01b**			**11b**
GPyMUXn. GPIOz =	**00b**	**01b**	**10b**	**11b**	**01b**	**10b**	**11b**	**11b**
	GPIO112			EM2BA1 (O)				
	GPIO113			EM2CAS (O)				
	GPIO114			EM2RAS (O)				
	GPIO115			EM2CS0 (O)				
	GPIO116			EM2CS2 (O)				
	GPIO117			EM2SDCKE (O)				
	GPIO118			EM2CLK (O)				
	GPIO119			EM2RNW (O)				
	GPIO120			EM2WE (O)				USB0PFLT
	GPIO121			EM2OE (O)				USB0EPEN
	GPIO122					SPISIMOC (I/O)	SD1_D1 (I)	
	GPIO123					SPISOMIC (I/O)	SD1_C1 (I)	
	GPIO124					SPICLKC (I/O)	SD1_D2 (I)	
	GPIO125					SPISTEC (I/O)	SD1_C2 (I)	
	GPIO126						SD1_D3 (I)	
	GPIO127						SD1_C3 (I)	
	GPIO128						SD1_D4 (I)	
	GPIO129						SD1_C4 (I)	
	GPIO130						SD2_D1 (I)	
	GPIO131						SD2_C1 (I)	
	GPIO132						SD2_D2 (I)	
	GPIO133/ AUXCLKIN						SD2_C2 (I)	
	GPIO134						SD2_D3 (I)	
	GPIO135					SCITXDA (O)	SD2_C3 (I)	
	GPIO136					SCIRXDA (I)	SD2_D4 (I)	
	GPIO137					SCITXDB (O)	SD2_C4 (I)	
	GPIO138					SCIRXDB (I)		
	GPIO139					SCIRXDC (I)		
	GPIO140					SCITXDC (O)		
	GPIO141					SCIRXDD (I)		
	GPIO142					SCITXDD (O)		
	GPIO143							
	GPIO144							
	GPIO145	EPWM1A (O)						
	GPIO146	EPWM1B (O)						
	GPIO147	EPWM2A (O)						
	GPIO148	EPWM2B (O)						
	GPIO149	EPWM3A (O)						
	GPIO150	EPWM3B (O)						
	GPIO151	EPWM4A (O)						
	GPIO152	EPWM4B (O)						
	GPIO153	EPWM5A (O)						
	GPIO154	EPWM5B (O)						
	GPIO155	EPWM6A (O)						
	GPIO156	EPWM6B (O)						
	GPIO157	EPWM7A (O)						
	GPIO158	EPWM7B (O)						
	GPIO159	EPWM8A (O)						
	GPIO160	EPWM8B (O)						
	GPIO161	EPWM9A (O)						
	GPIO162	EPWM9B (O)						

Table 8-7. GPIO Muxed Pins[1][2] (continued)

	GPIO Mux Selection							
GPIO Index	**0, 4, 8, 12**	**1**	**2**	**3**	**5**	**6**	**7**	**15**
GPyGMUXn. GPIOz =	**00b, 01b, 10b, 11b**	**00b**			**01b**			**11b**
GPyMUXn. GPIOz =	**00b**	**01b**	**10b**	**11b**	**01b**	**10b**	**11b**	**11b**
	GPIO163	EPWM10A (O)						
	GPIO164	EPWM10B (O)						
	GPIO165	EPWM11A (O)						
	GPIO166	EPWM11B (O)						
	GPIO167	EPWM12A (O)						
	GPIO168	EPWM12B (O)						

For example, the multiplexing for the GPIO 6 pin is controlled by writing toGPAGMUX[13:12] and GPAMUX[13:12]. By writing to these bits, GPIO 6 can be configured as either ageneral-purpose digital I/O or one of four different peripheral functions. The options are shown inTable 8-8.

Table 8-8. GPIO and Peripheral Muxing

GPAGMUX1[13:12]	GPAMUX1[13:12]	Pin functionality
00	00	GPIO6
00	01	EPWM4A
00	10	OUTPUTXBAR4
00	11	EXTSYNCOUT
01	00	GPIO6
01	01	EQEP3A
01	10	CANB_TX
01	11	
10	00	GPIO6
10	01	
10	10	
10	11	
11	00	GPIO6
11	01	
11	10	
11	11	

The devices have different multiplexing schemes. If a peripheral is not available on a particular device, that mux selection is reserved on that device and should not be used.

NOTE: If you select a reserved GPIO mux configuration that is not mapped to either a peripheral or GPIO mode, the state of the pin will be undefined and the pin may be driven. Unimplemented configurations are for future expansion and must not be selected. In the device mux table (see datasheet), these options are indicated as Reserved or left blank.

Some peripherals can be assigned to more than one pin via the mux registers. For example, OUTPUTXBAR1 can be assigned to GPIOs 2, 24, 34, or 58, depending on individual system requirements. An example of this is shown in Table 8-9.

Table 8-9. Peripheral Muxing (multiple pins assigned)

GMUX Configuration	MUX Configuration	
Choice 1 GPIO2	GPAGMUX1[5:4]=01	GPAMUX1[5:4]=01
or Choice 2 GPIO24	GPAGMUX2[17:16]=00	GPAMUX2[17:16]=01
or Choice 3 GPIO34	GPBGMUX1[5:4]=00	GPBMUX1[5:4]=01
or Choice 4 GPIO58	GPBGMUX2[21:20]=01	GPBMUX2[21:20]=01

If none, or more then one, of the GPIO pins are configured as peripheral input pins, then that GPIO will be set to a hard-wired default value.

8.8 Internal Pullup Configuration Requirements

On reset, GPIOs are in input mode and have the internal pullups disabled. An un-driven input can float to a mid-rail voltage and cause wasted shoot-through current on the input buffer. The user should always put each GPIO in one of these configurations:

- Input mode and driven on the board by another component to a level above V_{ih} or below V_{il}
- Input mode with GPIO internal pullup enabled
- Output mode

On devices with lesser pin count packages, pull-ups on unbonded GPIOs are by default enabled to prevent floating inputs. The user should take care to avoid disabling these pullups in their application code.

On devices in the 176 PTPor 100 PZP packages, the pullups for any internally unbonded GPIO must be enabled to prevent floating inputs. TI has provided functions in controlSUITE/C2000Ware which users can call to enable the pullup on any unbonded GPIO for the package they are using. This function, GPIO_EnabledUnbondedIOPullups(), resides in the (Device)_Sysctrl.c file and is called by default from InitSysCtrl(). The user should take care to avoid disabling these pullups in their application code.