6.3 Memory

6.3.1 C28x Memory Map

Both C28x CPUs on the device have the same memory map except where noted in Table 6-1. The GSx_RAM (Global Shared RAM) should be assigned to either CPU by the GSxMSEL register. Memories accessible by the CLA or DMA (direct memory access) are noted as well.

Table 6-1. C28x Memory Map

MEMORY	SIZE	START ADDRESS	END ADDRESS	CLA ACCESS	DMA ACCESS
M0 RAM	1K × 16	0x0000 0000	0x0000 03FF		
M1 RAM	1K × 16	0x0000 0400	0x0000 07FF		
PieVectTable	512 × 16	0x0000 0D00	0x0000 0EFF		
CPUx.CLA1 to CPUx MSGRAM	128 × 16	0x0000 1480	0x0000 14FF	Yes	
CPUx to CPUx.CLA1 MSGRAM	128 × 16	0x0000 1500	0x0000 157F	Yes	
UPP TX MSG RAM	512 × 16	0x0000 6C00	0x0000 6DFF	Yes	
UPP RX MSG RAM	512 × 16	0x0000 6E00	0x0000 6FFF	Yes	
LS0 RAM	2K × 16	0x0000 8000	0x0000 87FF	Yes	
LS1 RAM	2K × 16	0x0000 8800	0x0000 8FFF	Yes	
LS2 RAM	2K × 16	0x0000 9000	0x0000 97FF	Yes	
LS3 RAM	2K × 16	0x0000 9800	0x0000 9FFF	Yes	
LS4 RAM	2K × 16	0x0000 A000	0x0000 A7FF	Yes	
LS5 RAM	2K × 16	0x0000 A800	0x0000 AFFF	Yes	
D0 RAM	2K × 16	0x0000 B000	0x0000 B7FF		
D1 RAM	2K × 16	0x0000 B800	0x0000 BFFF		
GS0 RAM(1)	4K × 16	0x0000 C000	0x0000 CFFF		Yes
GS1 RAM(1)	4K × 16	0x0000 D000	0x0000 DFFF		Yes
GS2 RAM(1)	4K × 16	0x0000 E000	0x0000 EFFF		Yes
GS3 RAM(1)	4K × 16	0x0000 F000	0x0000 FFFF		Yes
GS4 RAM(1)	4K × 16	0x0001 0000	0x0001 0FFF		Yes
GS5 RAM(1)	4K × 16	0x0001 1000	0x0001 1FFF		Yes
GS6 RAM(1)	4K × 16	0x0001 2000	0x0001 2FFF		Yes
GS7 RAM(1)	4K × 16	0x0001 3000	0x0001 3FFF		Yes
GS8 RAM(1)	4K × 16	0x0001 4000	0x0001 4FFF		Yes
GS9 RAM(1)	4K × 16	0x0001 5000	0x0001 5FFF		Yes
GS10 RAM(1)	4K × 16	0x0001 6000	0x0001 6FFF		Yes
GS11 RAM(1)	4K × 16	0x0001 7000	0x0001 7FFF		Yes
GS12 RAM(1)(2)	4K × 16	0x0001 8000	0x0001 8FFF		Yes
GS13 RAM(1)(2)	4K × 16	0x0001 9000	0x0001 9FFF		Yes
GS14 RAM(1)(2)	4K × 16	0x0001 A000	0x0001 AFFF		Yes
GS15 RAM(1)(2)	4K × 16	0x0001 B000	0x0001 BFFF		Yes
CPU2 to CPU1 MSGRAM(1)	1K × 16	0x0003 F800	0x0003 FBFF		Yes
CPU1 to CPU2 MSGRAM(1)	1K × 16	0x0003 FC00	0x0003 FFFF		Yes
CAN A Message RAM(1)	2K × 16	0x0004 9000	0x0004 97FF		
CAN B Message RAM(1)	2K × 16	0x0004 B000	0x0004 B7FF		
Flash	256K × 16	0x0008 0000	0x000B FFFF		
Secure ROM	32K × 16	0x003F 0000	0x003F 7FFF		
Boot ROM	32K × 16	0x003F 8000	0x003F FFBF		
Vectors	64 × 16	0x003F FFC0	0x003F FFFF		

(1) Shared between CPU subsystems.
(2) Available only on F28379D, F28377D, and F28375D.

6.3.2 Flash Memory Map

On the F28379D, F28377D, and F28375D devices, each CPU has its own flash bank [512KB (256KW)], the total flash for each device is 1MB (512KW). Only one bank can be programmed or erased at a time and the code to program the flash should be executed out of RAM. Table 6-2 shows the addresses of flash sectors on CPU1 and CPU2 for F28379D, F28377D, and F28375D.

Table 6-2. Addresses of Flash Sectors on CPU1 and CPU2 for F28379D, F28377D, and F28375D

SECTOR	SIZE	START ADDRESS	END ADDRESS
OTP Sectors			
TI OTP	1K × 16	0x0007 0000	0x0007 03FF
User configurable DCSM OTP	1K × 16	0x0007 8000	0x0007 83FF
Sectors			
Sector A	8K × 16	0x0008 0000	0x0008 1FFF
Sector B	8K × 16	0x0008 2000	0x0008 3FFF
Sector C	8K × 16	0x0008 4000	0x0008 5FFF
Sector D	8K × 16	0x0008 6000	0x0008 7FFF
Sector E	32K × 16	0x0008 8000	0x0008 FFFF
Sector F	32K × 16	0x0009 0000	0x0009 7FFF
Sector G	32K × 16	0x0009 8000	0x0009 FFFF
Sector H	32K × 16	0x000A 0000	0x000A 7FFF
Sector I	32K × 16	0x000A 8000	0x000A FFFF
Sector J	32K × 16	0x000B 0000	0x000B 7FFF
Sector K	8K × 16	0x000B 8000	0x000B 9FFF
Sector L	8K × 16	0x000B A000	0x000B BFFF
Sector M	8K × 16	0x000B C000	0x000B DFFF
Sector N	8K ×16	0x000B E000	0x000B FFFF
Flash ECC Locations			
TI OTP ECC	128 × 16	0x0107 0000	0x0107 007F
User-configurable DCSM OTP ECC	128 × 16	0x0107 1000	0x0107 107F
Flash ECC	32K × 16	0x0108 0000	0x0108 7FFF