Table 3-2. PIE Channel Mapping

	INTx.1	INTx.2	INTx.3	INTx.4	INTx.5	INTx.6	INTx.7	INTx.8	INTx.9	INTx.10	INTx.11	INTx.12	INTx.13	INTx.14	INTx.15	INTx.16
INT1.y	ADCA1	ADCB1	ADCC1	XINT1	XINT2	ADCD1	TIMER0	WAKE/ WDINT	I2CA	SYS_ ERR	ECAT SYNC0 (CPU1 only)	ECAT INTn (CPU1 only)	CIPC0	CIPC1	CIPC2	CIPC3
INT2.y	EPWM1_ TZ	EPWM2_ TZ	EPWM3_ TZ	EPWM4_ TZ	EPWM5_ TZ	EPWM6_ TZ	EPWM7_ TZ	EPWM8_ TZ	EPWM9_ TZ	EPWM10_ TZ	EPWM11_ TZ	EPWM12_ TZ	EPWM13_ TZ	EPWM14_ TZ	EPWM15_ TZ	EPWM16_ TZ
INT3.y	EPWM1	EPWM2	EPWM3	EPWM4	EPWM5	EPWM6	EPWM7	EPWM8	EPWM9	EPWM10	EPWM11	EPWM12	EPWM13	EPWM14	EPWM15	EPWM16
INT4.y	ECAP1	ECAP2	ECAP3	ECAP4	ECAP5	ECAP6	ECAP7	-	FSITXA_ INT1	FSITXA_ INT2	FSITXB_ INT1	FSITXB_ INT2	FSIRXA_ INT1	FSIRXA_ INT2	FSIRXB_ INT1	FSIRXB_ INT2
INT5.y	EQEP1	EQEP2	EQEP3	-	CLB1	CLB2	CLB3	CLB4	SDFM1	SDFM2	ECAT RSTINTn (CPU1 only)	ECAT SYNC1 (CPU1 only)	SDFM1 DR1	SDFM1 DR2	SDFM1 DR3	SDFM1 DR4
INT6.y	SPIA_RX	SPIA_TX	SPIB_RX	SPIB_TX	MCBSPA_ RX	MCBSPA_ TX	MCBSPB_ RX	MCBSPB_ TX	SPIC_RX	SPIC_TX	SPID_RX	SPID_TX	SDFM2 DR1	SDFM2 DR2	SDFM2 DR3	SDFM2 DR4
INT7.y	DMA_CH1	DMA_CH2	DMA_CH3	DMA_CH4	DMA_CH5	DMA_CH6	-	-	FSIRXC_ INT1	FSIRXC_ INT2	FSIRXD_ INT1	FSIRXD_ INT2	FSIRXE_ INT1	FSIRXE_ INT2	FSIRXF_ INT1	FSIRXF_ INT2
INT8.y	I2CA	I2CA_ FIFO	I2CB	I2CB_ FIFO	SCIC_RX	SCIC_TX	SCID_RX	SCID_TX	FSIRXG_ INT1	FSIRXG_ INT2	FSIRXH_ INT1	FSIRXH_ INT2	CLB5	CLB6	CLB7	CLB8
INT9.y	SCIA_RX	SCIA_TX	SCIB_RX	SCIB_TX	CANA_0	CANA_1	CANB_0	CANB_1	MCANSS_ INT0 (CPU1 only)	MCANSS_ INT1 (CPU1 only)	MCANSS_ ECC_ CORR_ PUL_INT (CPU1 only)	MCANSS_ WAKE_ AND_TS_ PLS_INT (CPU1 only)	PMBUSA	CM_ STATUS (CPU1 only)	USBA (CPU1 only)	-
INT10.y	ADCA_ EVT	ADCA2	ADCA3	ADCA4	ADCB_ EVT	ADCB2	ADCB3	ADCB4	ADCC_EVT	ADCC2	ADCC3	ADCC4	ADCD_EVT	ADCD2	ADCD3	ADCD4
INT11.y	CLA1_1	CLA1_2	CLA1_3	CLA1_4	CLA1_5	CLA1_6	CLA1_7	CLA1_8	CMTOCPUx IPCINTR0	CMTOCPUx IPCINTR1	CMTOCPUx IPCINTR2	CMTOCPUx IPCINTR3	CMTOCPUx IPCINTR4	CMTOCPUx IPCINTR5	CMTOCPUx IPCINTR6	CMTOCPUx IPCINTR7
INT12.y	XINT3	XINT4	XINT5	MPOST	FMC. DONE	VCU	FPU OVER FLOW	FPU UNDER FLOW	-	ECAP6 INT2	ECAP7 INT2	-	CPUxCRC_ INT	CLA1CRC_ INT	CLA OVER FLOW	CLA UNDER FLOW

Note: Cells marked "-" are Reserved. CPUx is CPU1 for CPU1 PIE and CPU2 for CPU2 PIE.

3.4.5.1 PIE Interrupt Priority

3.4.5.1.1 Channel Priority

For every PIE group, the low number channels in the group have the highest priority. For instance in PIE group 1, channel 1.1 has priority over channel 1.3. If those two enabled interrupts occurred simultaneously, channel 1.1 will be serviced first with channel 1.3 left pending. Once the ISR for channel 1.1 completes and provided there are no other enabled and pending interrupts for PIE group 1, channel 1.3 will be serviced. However, for the CPU to service any more interrupts from a PIE group, PIEACK for the group must be cleared. For this specific example, in order for channel 1.3 to be serviced, channel 1.1's ISR has to clear PIEACK for group 1.

The following example describes an alternative scenario: channel 1.1 is currently being serviced by the CPU, channel 1.3 is pending and before channel 1.1's ISR completes, channel 1.2 which is enabled also comes in. Since channel 1.2 has a higher priority than channel 1.3, the CPU will service channel 1.2 and channel 1.3 will still be left pending. Using the steps from the Interrupt Entry Sequence Section 3.4.2.4, channel 1.2 interrupt can happen as late as step 10 (The CPU fetches the ISR vector from the PIE. PIEIFRx.y is cleared) and it will still be serviced ahead of channel 1.3.

3.4.5.1.2 Group Priority

Generally, the lowest channel in the lowest PIE group has the highest priority. An example of this is channels 1.1 and 2.1. Those two channels have the highest priority in their respective groups. If the interrupts for those two enabled channels happened simultaneously and provided there are no other enabled and pending interrupts, channel 1.1 will be serviced first by the CPU with channel 2.1 left pending.

However, there are cases where channel priority supersedes group priority. This special case happens depending on which step the CPU is currently at in the Interrupt Entry Sequence Section 3.4.2.4.

The following illustrates an example of this special case.

The CPU is about to service channel 2.3 and is currently going through the steps in the Interrupt Entry Sequence Section 3.4.2.4.

1. As the CPU reaches step 10 (The CPU fetches the ISR vector from the PIE. PIEIFRx.y is cleared), two enabled interrupts: channel 1.1 and channel 2.1 come in.
2. Due to channel priority, channel 2.1 will be serviced ahead of channel 2.3. However, group priority dictates that channel 1.1 be serviced ahead of channels 2.1 and 2.3.
3. Channel priority supersedes here and channel 2.1 will be serviced ahead of 1.1 and 2.3.
4. After channel 2.1 completes, channel 1.1 is serviced followed by channel 2.3.

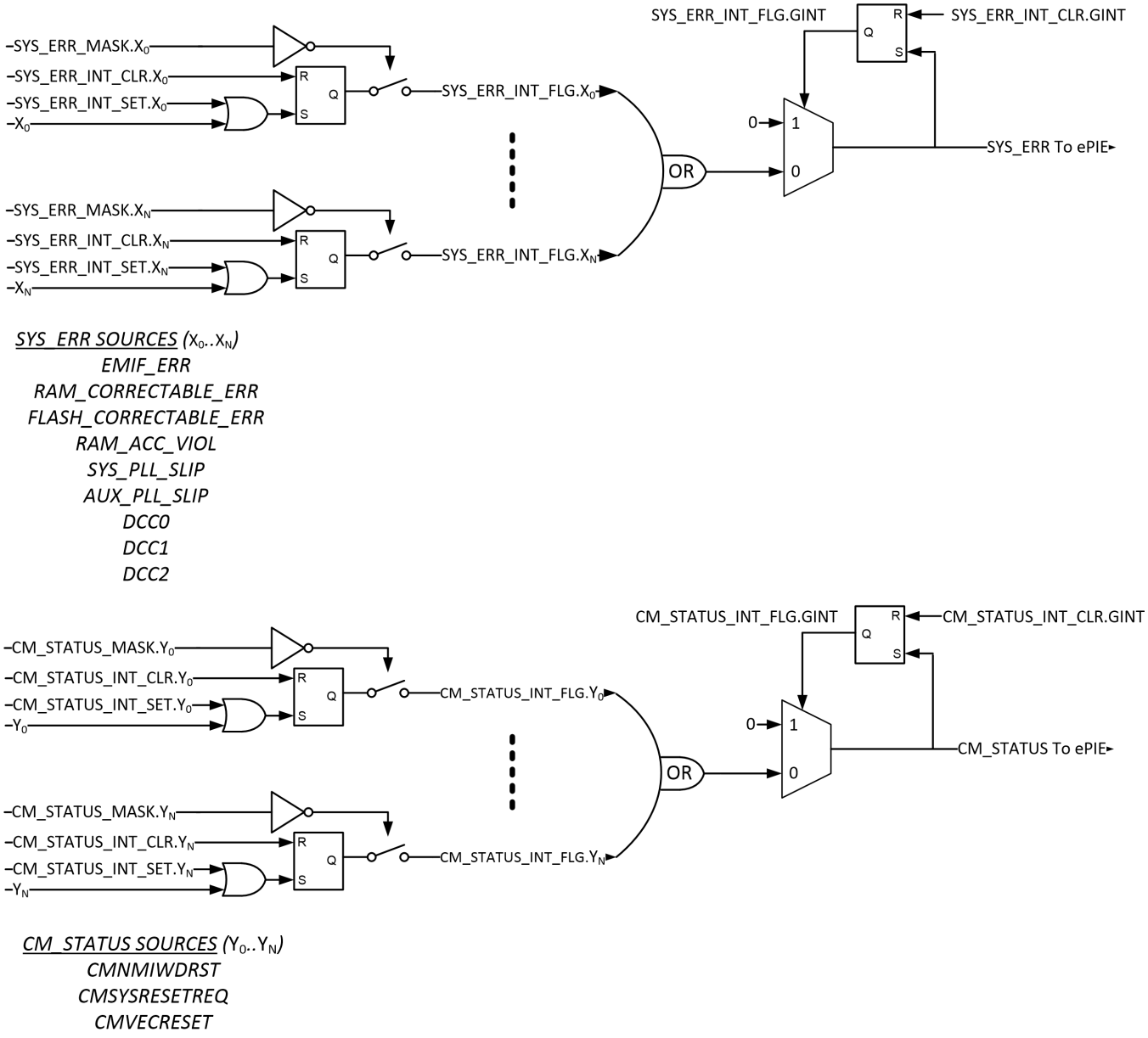
Group priority is only guaranteed if no interrupts are currently being serviced, that is, the Interrupt Entry Sequence Section 3.4.2.4 is not executing.

3.4.6 System Error and CM Status Interrupts

SYS_ERR and CM_STATUS consolidate several sources of interrupts. These sources set the respective bit in the SYS_ERR_INT_FLG and CM_STATUS_INT_FLG registers. Any set bit in the SYS_ERR_INT_FLG and CM_STATUS_INT_FLG registers will also set the GINT (Global Interrupt) bit. GINT has to be cleared before anymore SYS_ERR or CM_STATUS interrupts are generated. If GINT is cleared with the source flags still set, another SYS_ERR or CM_STATUS interrupt will be fired, therefore it is recommended to clear the source flags before clearing GINT.

Figure 3-3 shows the sources for SYS_ERR and CM_STATUS interrupts.

Figure 3-3. System Error and CM Status Interrupt Sources



3.4.7 Vector Tables

Table 3-3 shows the CPU interrupt vector table. The vectors for INT1 – INT12 are not used in this device. The reset vector is fetched from the boot ROM instead of from this table.

Table 3-3. CPU Interrupt Vectors

Name	Vector ID	Address	Size (x16)	Description	Core priority	ePIE group Priority
Reset	0	0x0000 0D00	2	Reset is always fetched from location 0x003F_FFC0 in Boot ROM	1 (Highest)	-
INT1	1	0x0000 0D02	2	Not used. See PIE Group 1	5	-
INT2	2	0x0000 0D04	2	Not used. See PIE Group 2	6	-
INT3	3	0x0000 0D06	2	Not used. See PIE Group 3	7	-

Table 3-3. CPU Interrupt Vectors (continued)

Name	Vector ID	Address	Size (x16)	Description	Core priority	ePIE group Priority
INT4	4	0x0000 0D08	2	Not used. See PIE Group 4	8	-
INT5	5	0x0000 0D0A	2	Not used. See PIE Group 5	9	-
INT6	6	0x0000 0D0C	2	Not used. See PIE Group 6	10	-
INT7	7	0x0000 0D0E	2	Not used. See PIE Group 7	11	-
INT8	8	0x0000 0D10	2	Not used. See PIE Group 8	12	-
INT9	9	0x0000 0D12	2	Not used. See PIE Group 9	13	-
INT10	10	0x0000 0D14	2	Not used. See PIE Group 10	14	-
INT11	11	0x0000 0D16	2	Not used. See PIE Group 11	15	-
INT12	12	0x0000 0D18	2	Not used. See PIE Group 12	16	-
INT13	13	0x0000 0D1A	2	CPU TIMER1 Interrupt	17	-
INT14	14	0x0000 0D1C	2	CPU TIMER2 Interrupt (for TI/RTOS use)	18	-
DATALOG	15	0x0000 0D1E	2	CPU Data Logging Interrupt	19 (lowest)	-
RTOSINT	16	0x0000 0D20	2	CPU Real-Time OS Interrupt	4	-
EMUINT	17	0x0000 0D22	2	CPU Emulation Interrupt	2	-
NMI	18	0x0000 0D24	2	Non-Maskable Interrupt	3	-
ILLEGAL	19	0x0000 0D26	2	Illegal Instruction (ITRAP)	-	-
USER 1	20	0x0000 0D28	2	User-Defined Trap	-	-
USER 2	21	0x0000 0D2A	2	User-Defined Trap	-	-
USER 3	22	0x0000 0D2C	2	User-Defined Trap	-	-
USER 4	23	0x0000 0D2E	2	User-Defined Trap	-	-
USER 5	24	0x0000 0D30	2	User-Defined Trap	-	-
USER 6	25	0x0000 0D32	2	User-Defined Trap	-	-
USER 7	26	0x0000 0D34	2	User-Defined Trap	-	-
USER 8	27	0x0000 0D36	2	User-Defined Trap	-	-
USER 9	28	0x0000 0D38	2	User-Defined Trap	-	-
USER 10	29	0x0000 0D3A	2	User-Defined Trap	-	-
USER 11	30	0x0000 0D3C	2	User-Defined Trap	-	-
USER 12	31	0x0000 0D3E	2	User-Defined Trap	-	-

Table 3-4 shows the Pie vector table.

Table 3-4. PIE Interrupt Vectors

Name	Vector ID	Address	Size (x16)	Description	Core priority	ePIE group Priority
PIE Group 1 Vectors - Muxed into CPU INT1						
INT1.1	32	0x0000 0D40	2	ADCA1 interrupt	5	1 (Highest)
INT1.2	33	0x0000 0D42	2	ADCB1 interrupt	5	2
INT1.3	34	0x0000 0D44	2	ADCC1 interrupt	5	3
INT1.4	35	0x0000 0D46	2	XINT1 interrupt	5	4
INT1.5	36	0x0000 0D48	2	XINT2 interrupt	5	5
INT1.6	37	0x0000 0D4A	2	ADCD1 interrupt	5	6
INT1.7	38	0x0000 0D4C	2	TIMER0 interrupt	5	7
INT1.8	39	0x0000 0D4E	2	WAKE/WD interrupt	5	8
INT1.9	128	0x0000 0E00	2	I2CA interrupt	5	9
INT1.10	129	0x0000 0E02	2	SYS_ERR interrupt	5	10
INT1.11	130	0x0000 0E04	2	ECAT SYNC0 interrupt (CPU1 only)	5	11
INT1.12	131	0x0000 0E06	2	ECAT interrupt n (CPU1 only)	5	12
INT1.13	132	0x0000 0E08	2	CIPC0 interrupt	5	13
INT1.14	133	0x0000 0E0A	2	CIPC1 interrupt	5	14
INT1.15	134	0x0000 0E0C	2	CIPC2 interrupt	5	15
INT1.16	135	0x0000 0E0E	2	CIPC3 interrupt	5	16 (Lowest)
PIE Group 2 Vectors - Muxed into CPU INT2						
INT2.1	40	0x0000 0D50	2	EPWM1_TZ interrupt	6	1 (Highest)
INT2.2	41	0x0000 0D52	2	EPWM2_TZ interrupt	6	2
INT2.3	42	0x0000 0D54	2	EPWM3_TZ interrupt	6	3
INT2.4	43	0x0000 0D56	2	EPWM4_TZ interrupt	6	4
INT2.5	44	0x0000 0D58	2	EPWM5_TZ interrupt	6	5
INT2.6	45	0x0000 0D5A	2	EPWM6_TZ interrupt	6	6
INT2.7	46	0x0000 0D5C	2	EPWM7_TZ interrupt	6	7
INT2.8	47	0x0000 0D5E	2	EPWM8_TZ interrupt	6	8
INT2.9	136	0x0000 0E10	2	EPWM9_TZ interrupt	6	9
INT2.10	137	0x0000 0E12	2	EPWM10_TZ interrupt	6	10
INT2.11	138	0x0000 0E14	2	EPWM11_TZ interrupt	6	11
INT2.12	139	0x0000 0E16	2	EPWM12_TZ interrupt	6	12
INT2.13	140	0x0000 0E18	2	EPWM13_TZ interrupt	6	13
INT2.14	141	0x0000 0E1A	2	EPWM14_TZ interrupt	6	14

Table 3-4. PIE Interrupt Vectors (continued)

Name	Vector ID	Address	Size (x16)	Description	Core priority	ePIE group Priority
INT2.15	142	0x0000 0E1C	2	EPWM15_TZ interrupt	6	15
INT2.16	143	0x0000 0E1E	2	EPWM16_TZ interrupt	6	16 (Lowest)
PIE Group 3 Vectors - Muxed into CPU INT3						
INT3.1	48	0x0000 0D60	2	EPWM1 interrupt	7	1 (Highest)
INT3.2	49	0x0000 0D62	2	EPWM2 interrupt	7	2
INT3.3	50	0x0000 0D64	2	EPWM3 interrupt	7	3
INT3.4	51	0x0000 0D66	2	EPWM4 interrupt	7	4
INT3.5	52	0x0000 0D68	2	EPWM5 interrupt	7	5
INT3.6	53	0x0000 0D6A	2	EPWM6 interrupt	7	6
INT3.7	54	0x0000 0D6C	2	EPWM7 interrupt	7	7
INT3.8	55	0x0000 0D6E	2	EPWM8 interrupt	7	8
INT3.9	144	0x0000 0E20	2	EPWM9 interrupt	7	9
INT3.10	145	0x0000 0E22	2	EPWM10 interrupt	7	10
INT3.11	146	0x0000 0E24	2	EPWM11 interrupt	7	11
INT3.12	147	0x0000 0E26	2	EPWM12 interrupt	7	12
INT3.13	148	0x0000 0E28	2	EPWM13 interrupt	7	13
INT3.14	149	0x0000 0E2A	2	EPWM14 interrupt	7	14
INT3.15	150	0x0000 0E2C	2	EPWM15 interrupt	7	15
INT3.16	151	0x0000 0E2E	2	EPWM16 interrupt	7	16 (Lowest)
PIE Group 4 Vectors - Muxed into CPU INT4						
INT4.1	56	0x0000 0D70	2	ECAP1 interrupt	8	1 (Highest)
INT4.2	57	0x0000 0D72	2	ECAP2 interrupt	8	2
INT4.3	58	0x0000 0D74	2	ECAP3 interrupt	8	3
INT4.4	59	0x0000 0D76	2	ECAP4 interrupt	8	4
INT4.5	60	0x0000 0D78	2	ECAP5 interrupt	8	5
INT4.6	61	0x0000 0D7A	2	ECAP6 interrupt	8	6
INT4.7	62	0x0000 0D7C	2	ECAP7 interrupt	8	7
INT4.8	63	0x0000 0D7E	2	Reserved	8	8
INT4.9	152	0x0000 0E30	2	FSITXA interrupt 1	8	9
INT4.10	153	0x0000 0E32	2	FSITXA interrupt 2	8	10
INT4.11	154	0x0000 0E34	2	FSITXB interrupt 1	8	11
INT4.12	155	0x0000 0E36	2	FSITXB interrupt 2	8	12
INT4.13	156	0x0000 0E38	2	FSIRXA interrupt 1	8	13
INT4.14	157	0x0000 0E3A	2	FSIRXA interrupt 2	8	14
INT4.15	158	0x0000 0E3C	2	FSIRXB interrupt 1	8	15

Table 3-4. PIE Interrupt Vectors (continued)

Name	Vector ID	Address	Size (x16)	Description	Core priority	ePIE group Priority
INT4.16	159	0x0000 0E3E	2	FSIRXB interrupt 2	8	16 (Lowest)
PIE Group 5 Vectors - Muxed into CPU INT5						
INT5.1	64	0x0000 0D80	2	EQEP1 interrupt	9	1 (Highest)
INT5.2	65	0x0000 0D82	2	EQEP2 interrupt	9	2
INT5.3	66	0x0000 0D84	2	EQEP3 interrupt	9	3
INT5.4	67	0x0000 0D86	2	Reserved	9	4
INT5.5	68	0x0000 0D88	2	CLB1 interrupt	9	5
INT5.6	69	0x0000 0D8A	2	CLB2 interrupt	9	6
INT5.7	70	0x0000 0D8C	2	CLB3 interrupt	9	7
INT5.8	71	0x0000 0D8E	2	CLB4 interrupt	9	8
INT5.9	160	0x0000 0E40	2	SDFM1 interrupt	9	9
INT5.10	161	0x0000 0E42	2	SDFM2 interrupt	9	10
INT5.11	162	0x0000 0E44	2	ECATRST interrupt n (CPU1 only)	9	11
INT5.12	163	0x0000 0E46	2	ECATSYNC1 interrupt (CPU1 only)	9	12
INT5.13	164	0x0000 0E48	2	SDFM1DR1 interrupt	9	13
INT5.14	165	0x0000 0E4A	2	SDFM1DR2 interrupt	9	14
INT5.15	166	0x0000 0E4C	2	SDFM1DR3 interrupt	9	15
INT5.16	167	0x0000 0E4E	2	SDFM1DR4 interrupt	9	16 (Lowest)
PIE Group 6 Vectors - Muxed into CPU INT6						
INT6.1	72	0x0000 0D90	2	SPIA_RX interrupt	10	1 (Highest)
INT6.2	73	0x0000 0D92	2	SPIA_TX interrupt	10	2
INT6.3	74	0x0000 0D94	2	SPIB_RX interrupt	10	3
INT6.4	75	0x0000 0D96	2	SPIB_TX interrupt	10	4
INT6.5	76	0x0000 0D98	2	MCBSPA_RX interrupt	10	5
INT6.6	77	0x0000 0D9A	2	MCBSPA_TX interrupt	10	6
INT6.7	78	0x0000 0D9C	2	MCBSPB_RX interrupt	10	7
INT6.8	79	0x0000 0D9E	2	MCBSPB_TX interrupt	10	8
INT6.9	168	0x0000 0E50	2	SPIC_RX interrupt	10	9
INT6.10	169	0x0000 0E52	2	SPIC_TX interrupt	10	10
INT6.11	170	0x0000 0E54	2	SPID_RX interrupt	10	11
INT6.12	171	0x0000 0E56	2	SPID_TX interrupt	10	12
INT6.13	172	0x0000 0E58	2	SDFM2DR1 interrupt	10	13

Table 3-4. PIE Interrupt Vectors (continued)

Name	Vector ID	Address	Size (x16)	Description	Core priority	ePIE group Priority
INT6.14	173	0x0000 0E5A	2	SDFM2DR2 interrupt	10	14
INT6.15	174	0x0000 0E5C	2	SDFM2DR3 interrupt	10	15
INT6.16	175	0x0000 0E5E	2	SDFM2DR4 interrupt	10	16 (Lowest)
PIE Group 7 Vectors - Muxed into CPU INT7						
INT7.1	80	0x0000 0DA0	2	DMA_CH1 interrupt	11	1 (Highest)
INT7.2	81	0x0000 0DA2	2	DMA_CH2 interrupt	11	2
INT7.3	82	0x0000 0DA4	2	DMA_CH3 interrupt	11	3
INT7.4	83	0x0000 0DA6	2	DMA_CH4 interrupt	11	4
INT7.5	84	0x0000 0DA8	2	DMA_CH5 interrupt	11	5
INT7.6	85	0x0000 0DAA	2	DMA_CH6 interrupt	11	6
INT7.7	86	0x0000 0DAC	2	Reserved	11	7
INT7.8	87	0x0000 0DAE	2	Reserved	11	8
INT7.9	176	0x0000 0E60	2	FSIRXC interrupt 1	11	9
INT7.10	177	0x0000 0E62	2	FSIRXC interrupt 2	11	10
INT7.11	178	0x0000 0E64	2	FSIRXD interrupt 1	11	11
INT7.12	179	0x0000 0E66	2	FSIRXD interrupt 2	11	12
INT7.13	180	0x0000 0E68	2	FSIRXE interrupt 1	11	13
INT7.14	181	0x0000 0E6A	2	FSIRXE interrupt 2	11	14
INT7.15	182	0x0000 0E6C	2	FSIRXF interrupt 1	11	15
INT7.16	183	0x0000 0E6E	2	FSIRXF interrupt 2	11	16 (Lowest)
PIE Group 8 Vectors - Muxed into CPU INT8						
INT8.1	88	0x0000 0DB0	2	I2CA interrupt	12	1 (Highest)
INT8.2	89	0x0000 0DB2	2	I2CA_FIFO interrupt	12	2
INT8.3	90	0x0000 0DB4	2	I2CB interrupt	12	3
INT8.4	91	0x0000 0DB6	2	I2CB_FIFO interrupt	12	4
INT8.5	92	0x0000 0DB8	2	SCIC_RX interrupt	12	5
INT8.6	93	0x0000 0DBA	2	SCIC_TX interrupt	12	6
INT8.7	94	0x0000 0DBC	2	SCID_RX interrupt	12	7
INT8.8	95	0x0000 0DBE	2	SCID_TX interrupt	12	8
INT8.9	184	0x0000 0E70	2	FSIRXG interrupt 1	12	9

Table 3-4. PIE Interrupt Vectors (continued)

Name	Vector ID	Address	Size (x16)	Description	Core priority	ePIE group Priority
INT8.10	185	0x0000 0E72	2	FSIRXG interrupt 2	12	10
INT8.11	186	0x0000 0E74	2	FSIRXH interrupt 1	12	11
INT8.12	187	0x0000 0E76	2	FSIRXH interrupt 2	12	12
INT8.13	188	0x0000 0E78	2	CLB5 interrupt	12	13
INT8.14	189	0x0000 0E7A	2	CLB6 interrupt	12	14
INT8.15	190	0x0000 0E7C	2	CLB7 interrupt	12	15
INT8.16	191	0x0000 0E7E	2	CLB8 interrupt	12	16 (Lowest)
PIE Group 9 Vectors - Muxed into CPU INT9						
INT9.1	96	0x0000 0DC0	2	SCIA_RX interrupt	13	1 (Highest)
INT9.2	97	0x0000 0DC2	2	SCIA_TX interrupt	13	2
INT9.3	98	0x0000 0DC4	2	SCIB_RX interrupt	13	3
INT9.4	99	0x0000 0DC6	2	SCIB_TX interrupt	13	4
INT9.5	100	0x0000 0DC8	2	CANA interrupt 0	13	5
INT9.6	101	0x0000 0DCA	2	CANA interrupt 1	13	6
INT9.7	102	0x0000 0DCC	2	CANB interrupt 0	13	7
INT9.8	103	0x0000 0DCE	2	CANB interrupt 1	13	8
INT9.9	192	0x0000 0E80	2	MCANSS interrupt 0 (CPU1 only)	13	9
INT9.10	193	0x0000 0E82	2	MCANSS interrupt 1 (CPU1 only)	13	10
INT9.11	194	0x0000 0E84	2	MCANSS_ECC_CORR_PUL interrupt (CPU1 only)	13	11
INT9.12	195	0x0000 0E86	2	MCANSS_WAKE_AND_TS_PLS interrupt (CPU1 only)	13	12
INT9.13	196	0x0000 0E88	2	PMBUSA interrupt	13	13
INT9.14	197	0x0000 0E8A	2	CM_STATUS interrupt (CPU1 only)	13	14
INT9.15	198	0x0000 0E8C	2	USBA interrupt (CPU1 only)	13	15
INT9.16	199	0x0000 0E8E	2	Reserved	13	16 (Lowest)
PIE Group 10 Vectors - Muxed into CPU INT10						
INT10.1	104	0x0000 0DD0	2	ADCA_EVT interrupt	14	1 (Highest)
INT10.2	105	0x0000 0DD2	2	ADCA2 interrupt	14	2
INT10.3	106	0x0000 0DD4	2	ADCA3 interrupt	14	3
INT10.4	107	0x0000 0DD6	2	ADCA4 interrupt	14	4
INT10.5	108	0x0000 0DD8	2	ADCB_EVT interrupt	14	5
INT10.6	109	0x0000 0DDA	2	ADCB2 interrupt	14	6

Table 3-4. PIE Interrupt Vectors (continued)

Name	Vector ID	Address	Size (x16)	Description	Core priority	ePIE group Priority
INT10.7	110	0x0000 0DDC	2	ADCB3 interrupt	14	7
INT10.8	111	0x0000 0DDE	2	ADCB4 interrupt	14	8
INT10.9	200	0x0000 0E90	2	ADCC_EVT interrupt	14	9
INT10.10	201	0x0000 0E92	2	ADCC2 interrupt	14	10
INT10.11	202	0x0000 0E94	2	ADCC3 interrupt	14	11
INT10.12	203	0x0000 0E96	2	ADCC4 interrupt	14	12
INT10.13	204	0x0000 0E98	2	ADCD_EVT interrupt	14	13
INT10.14	205	0x0000 0E9A	2	ADCD2 interrupt	14	14
INT10.15	206	0x0000 0E9C	2	ADCD3 interrupt	14	15
INT10.16	207	0x0000 0E9E	2	ADCD4 interrupt	14	16 (Lowest)
PIE Group 11 Vectors - Muxed into CPU INT11						
INT11.1	112	0x0000 0DE0	2	CLA1_1 interrupt	15	1 (Highest)
INT11.2	113	0x0000 0DE2	2	CLA1_2 interrupt	15	2
INT11.3	114	0x0000 0DE4	2	CLA1_3 interrupt	15	3
INT11.4	115	0x0000 0DE6	2	CLA1_4 interrupt	15	4
INT11.5	116	0x0000 0DE8	2	CLA1_5 interrupt	15	5
INT11.6	117	0x0000 0DEA	2	CLA1_6 interrupt	15	6
INT11.7	118	0x0000 0DEC	2	CLA1_7 interrupt	15	7
INT11.8	119	0x0000 0DEE	2	CLA1_8 interrupt	15	8
INT11.9	208	0x0000 0EA0	2	CMTOCPUx IPC interrupt 0	15	9
INT11.10	209	0x0000 0EA2	2	CMTOCPUx IPC interrupt 1	15	10
INT11.11	210	0x0000 0EA4	2	CMTOCPUx IPC interrupt 2	15	11
INT11.12	211	0x0000 0EA6	2	CMTOCPUx IPC interrupt 3	15	12
INT11.13	212	0x0000 0EA8	2	CMTOCPUx IPC interrupt 4	15	13
INT11.14	213	0x0000 0EAA	2	CMTOCPUx IPC interrupt 5	15	14
INT11.15	214	0x0000 0EAC	2	CMTOCPUx IPC interrupt 6	15	15
INT11.16	215	0x0000 0EAE	2	CMTOCPUx IPC interrupt 7	15	16 (Lowest)
PIE Group 12 Vectors - Muxed into CPU INT12						
INT12.1	120	0x0000 0DF0	2	XINT3 interrupt	16	1 (Highest)
INT12.2	121	0x0000 0DF2	2	XINT4 interrupt	16	2
INT12.3	122	0x0000 0DF4	2	XINT5 interrupt	16	3
INT12.4	123	0x0000 0DF6	2	MPOST interrupt	16	4
INT12.5	124	0x0000 0DF8	2	FMC.DONE interrupt	16	5
INT12.6	125	0x0000 0DFA	2	VCU interrupt	16	6
INT12.7	126	0x0000 0DFC	2	FPU OVERFLOW interrupt	16	7
INT12.8	127	0x0000 0DFE	2	FPU UNDERFLOW interrupt	16	8

Table 3-4. PIE Interrupt Vectors (continued)

Name	Vector ID	Address	Size (x16)	Description	Core priority	ePIE group Priority
INT12.9	216	0x0000 0EB0	2	Reserved	16	9
INT12.10	217	0x0000 0EB2	2	ECAP6 interrupt	16	10
INT12.11	218	0x0000 0EB4	2	ECAP7 interrupt	16	11
INT12.12	219	0x0000 0EB6	2	Reserved	16	12
INT12.13	220	0x0000 0EB8	2	CPUxCRC interrupt	16	13
INT12.14	221	0x0000 0EBA	2	CLA1CRC interrupt	16	14
INT12.15	222	0x0000 0EBC	2	CLA OVERFLOW interrupt	16	15
INT12.16	223	0x0000 0EBE	2	CLA UNDERFLOW interrupt	16	16 (Lowest)

3.5 Exceptions and Non-Maskable Interrupts

This section describes system-level error conditions that can trigger a non-maskable interrupt (NMI). The interrupt allows the application to respond to the error.

3.5.1 Configuring and Using NMIs

Each CPU subsystem has its own NMI module. This section will provide detail of NMI on C28x subsystems. An incoming NMI sets a status bit in the NMIFLG register and starts the NMI watchdog counter. This counter is clocked by the SYSCLK, and if it reaches the value programmed in NMIWDPRD register, it triggers an NMI watchdog reset (NMIWDRS). To prevent this, the NMI handler must clear the flag bit using the NMIFLGCLR register. Once all flag bits are clear, the NMIINT bit in the NMIFLG register should be cleared to allow future NMIs to be taken.

The NMI module is enabled by the boot ROM during the startup process. To respond to NMIs, an NMI handler vector must be written to the PIE vector table.

3.5.2 Emulation Considerations

The NMI watchdog counter behaves as follows under debug conditions:

CPU Suspended	When the CPU is suspended, the NMI watchdog counter will be suspended.
Run-Free Mode	When the CPU is placed in run-free mode, the NMI watchdog counter will resume operation as normal.
Real-Time Single-Step Mode	When the CPU is in real-time single-step mode, the NMI watchdog counter will be suspended. The counter remains suspended even within real-time interrupts.
Real-Time Run-Free Mode	When the CPU is in real-time run-free mode, the NMI watchdog counter operates as normal.