6.2 Pin Attributes

Table 6-1. Pin Attributes

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
ANALOG					
ADCIN14		T4	44	I	Input 14 to all ADCs. This pin can be used as a general purpose ADCIN pin or it can be used to calibrate all ADCs together (either single-ended or differential) from an external reference
CMPIN4P				I	Comparator 4 positive input
ADCIN15		U4	45	I	Input 15 to all ADCs. This pin can be used as a general purpose ADCIN pin or it can be used to calibrate all ADCs together (either single-ended or differential) from an external reference
CMPIN4N				I	Comparator 4 negative input
ADCINA0		U1	43	I	ADC-A Input 0. There is a 50-kΩ internal pulldown on this pin in both an ADC input or DAC output mode which cannot be disabled.
DACOUTA				O	Buffered DAC-A Output.
ADCINA1		T1	42	I	ADC-A Input 1. There is a 50-kΩ internal pulldown on this pin in both an ADC input or DAC output mode which cannot be disabled.
DACOUTB				O	Buffered DAC-B Output.
ADCINA2		U2	41	I	ADC-A Input 2
CMPIN1P				I	Comparator 1 positive input
ADCINA3		T2	40	I	ADC-A Input 3
CMPIN1N				I	Comparator 1 negative input
ADCINA4		U3	39	I	ADC-A Input 4
CMPIN2P				I	Comparator 2 positive input
ADCINA5		T3	38	I	ADC-A Input 5
CMPIN2N				I	Comparator 2 negative input
ADCINB0		V2	46	I	ADC-B Input 0. There is a 100-pF capacitor to VSSA on this pin whether used for ADC input or DAC reference which cannot be disabled. If this pin is being used as a reference for the on-chip DACs, place at least a 1-µF capacitor on this pin.
VDAC				I	Optional external reference voltage for on-chip DACs.
ADCINB1		W2	47	I	ADC-B Input 1. There is a 50-kΩ internal pulldown on this pin in both an ADC input or DAC output mode which cannot be disabled.
DACOUTC				O	Buffered DAC-C Output.
ADCINB2		V3	48	I	ADC-B Input 2
CMPIN3P				I	Comparator 3 positive input
ADCINB3		W3	49	I	ADC-B Input 3
CMPIN3N				I	Comparator 3 negative input
ADCINB4		V4		I	ADC-B Input 4
ADCINB5		W4		I	ADC-B Input 5
ADCINC2		R3	31	I	ADC-C Input 2
CMPIN6P				I	Comparator 6 positive input
ADCINC3		P3	30	I	ADC-C Input 3
CMPIN6N				I	Comparator 6 negative input

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
ADCINC4		R4	29	I	ADC-C Input 4
CMPIN5P				I	Comparator 5 positive input
ADCINC5		P4		I	ADC-C Input 5
CMPIN5N				I	Comparator 5 negative input
ADCIND0		T5	56	I	ADC-D Input 0
CMPIN7P				I	Comparator 7 positive input
ADCIND1		U5	57	I	ADC-D Input 1
CMPIN7N				I	Comparator 7 negative input
ADCIND2		T6	58	I	ADC-D Input 2
CMPIN8P				I	Comparator 8 positive input
ADCIND3		U6	59	I	ADC-D Input 3
CMPIN8N				I	Comparator 8 negative input
ADCIND4		T7	60	I	ADC-D Input 4
ADCIND5		U7		I	ADC-D Input 5
VREFHIA		V1	37	I	ADC-A high reference. This voltage must be driven into the pin from external circuitry. Place at least a 2.2-µF capacitor on this pin for the 12-bit mode, or at least a 22-µF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the VREFHIA and VREFLOA pins. NOTE: Do not load this pin externally
VREFHIB		W5	53	I	ADC-B high reference. This voltage must be driven into the pin from external circuitry. Place at least a 2.2-µF capacitor on this pin for the 12-bit mode, or at least a 22-µF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the VREFHIB and VREFLOB pins. NOTE: Do not load this pin externally
VREFHIC		R1	35	I	ADC-C high reference. This voltage must be driven into the pin from external circuitry. Place at least a 2.2-µF capacitor on this pin for the 12-bit mode, or at least a 22-µF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the VREFHIC and VREFLOC pins. NOTE: Do not load this pin externally
VREFHID		V5	55	I	ADC-D high reference. This voltage must be driven into the pin from external circuitry. Place at least a 2.2-µF capacitor on this pin for the 12-bit mode, or at least a 22-µF capacitor for the 16-bit mode. This capacitor should be placed as close to the device as possible between the VREFHID and VREFLOD pins. NOTE: Do not load this pin externally
VREFLOA		R2	33	I	ADC-A Low Reference
VREFLOB		V6	50	I	ADC-B Low Reference
VREFLOC		P2	32	I	ADC-C Low Reference
VREFLOD		W6	51	I	ADC-D Low Reference

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO					
GPIO0	0, 4, 8, 12	C8	160	I/O	General-Purpose Input Output 0
EPWM1A	1			O	ePWM-1 Output A (High-res available on ePWM1-8)
I2CA_SDA	6			I/OD	I2C-A Open-Drain Bidirectional Data
CM-I2CA_SDA	9			I/OD	CM-I2C-A Open-Drain Bidirectional Data
ESC_GPI0	10			I	EtherCAT General-Purpose Input 0
FSITXA_D0	13			O	FSITX-A Data Output 0
GPIO1	0, 4, 8, 12	D8	161	I/O	General-Purpose Input Output 1
EPWM1B	1			O	ePWM-1 Output B (High-res available on ePWM1-8)
MFSRB	3			I	McBSP-B Receive Frame Sync
I2CA_SCL	6			I/OD	I2C-A Open-Drain Bidirectional Clock
CM-I2CA_SCL	9			I/OD	CM-I2C-A Open-Drain Bidirectional Clock
ESC_GPI1	10			I	EtherCAT General-Purpose Input 1
FSITXA_D1	13			O	FSITX-A Data Output 1
GPIO2	0, 4, 8, 12	A7	162	I/O	General-Purpose Input Output 2
EPWM2A	1			O	ePWM-2 Output A (High-res available on ePWM1-8)
OUTPUTXBAR1	5			O	Output X-BAR Output 1
I2CB_SDA	6			I/OD	I2C-B Open-Drain Bidirectional Data
ESC_GPI2	10			I	EtherCAT General-Purpose Input 2
FSITXA_CLK	13			O	FSITX-A Output Clock
GPIO3	0, 4, 8, 12	B7	163	I/O	General-Purpose Input Output 3
EPWM2B	1			O	ePWM-2 Output B (High-res available on ePWM1-8)
OUTPUTXBAR2	2, 5			O	Output X-BAR Output 2
MCLKRB	3			I	McBSP-B Receive Clock
I2CB_SCL	6			I/OD	I2C-B Open-Drain Bidirectional Clock
ESC_GPI3	10			I	EtherCAT General-Purpose Input 3
FSIRXA_D0	13			I	FSIRX-A Data Input 0
GPIO4	0, 4, 8, 12	C7	164	I/O	General-Purpose Input Output 4
EPWM3A	1			O	ePWM-3 Output A (High-res available on ePWM1-8)
OUTPUTXBAR3	5			O	Output X-BAR Output 3
CANA_TX	6			O	CAN-A Transmit
MCAN_TX	9			O	CAN/CAN-FD Transmit
ESC_GPI4	10			I	EtherCAT General-Purpose Input 4
FSIRXA_D1	13			I	FSIRX-A Data Input 1
GPIO5	0, 4, 8, 12	D7	165	I/O	General-Purpose Input Output 5
EPWM3B	1			O	ePWM-3 Output B (High-res available on ePWM1-8)
MFSRA	2			I	McBSP-A Receive Frame Sync
OUTPUTXBAR3	3			O	Output X-BAR Output 3
CANA_RX	6			I	CAN-A Receive
MCAN_RX	9			I	CAN/CAN-FD Receive
ESC_GPI5	10			I	EtherCAT General-Purpose Input 5
FSIRXA_CLK	13			I	FSIRX-A Input Clock

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO6	0, 4, 8, 12	A6	166	I/O	General-Purpose Input Output 6
EPWM4A	1			O	ePWM-4 Output A (High-res available on ePWM1-8)
OUTPUTXBAR4	2			O	Output X-BAR Output 4
EXTSYNCOUT	3			O	External ePWM Synchronization Pulse
EQEP3_A	5			I	eQEP-3 Input A
CANB_TX	6			O	CAN-B Transmit
ESC_GPI6	10			I	EtherCAT General-Purpose Input 6
FSITXB_D0	13			O	FSITX-B Data Output 0
GPIO7	0, 4, 8, 12	B6	167	I/O	General-Purpose Input Output 7
EPWM4B	1			O	ePWM-4 Output B (High-res available on ePWM1-8)
MCLKRA	2			I	McBSP-A Receive Clock
OUTPUTXBAR5	3			O	Output X-BAR Output 5
EQEP3_B	5			I	eQEP-3 Input B
CANB_RX	6			I	CAN-B Receive
ESC_GPI7	10			I	EtherCAT General-Purpose Input 7
FSITXB_D1	13			O	FSITX-B Data Output 1
GPIO8	0, 4, 8, 12	G2	18	I/O	General-Purpose Input Output 8
EPWM5A	1			O	ePWM-5 Output A (High-res available on ePWM1-8)
CANB_TX	2			O	CAN-B Transmit
ADCSOCAO	3			O	ADC Start of Conversion A Output for External ADC (from ePWM modules)
EQEP3_STROBE	5			I/O	eQEP-3 Strobe
SCIA_TX	6			O	SCI-A Transmit Data
MCAN_TX	9			O	CAN/CAN-FD Transmit
ESC_GPO0	10			O	EtherCAT General-Purpose Output 0
FSITXB_CLK	13			O	FSITX-B Output Clock
FSITXA_D1	14			O	FSITX-A Data Output 1
FSIRXA_D0	15			I	FSIRX-A Data Input 0
GPIO9	0, 4, 8, 12	G3	19	I/O	General-Purpose Input Output 9
EPWM5B	1			O	ePWM-5 Output B (High-res available on ePWM1-8)
SCIB_TX	2			O	SCI-B Transmit Data
OUTPUTXBAR6	3			O	Output X-BAR Output 6
EQEP3_INDEX	5			I/O	eQEP-3 Index
SCIA_RX	6			I	SCI-A Receive Data
ESC_GPO1	10			O	EtherCAT General-Purpose Output 1
FSIRXB_D0	13			I	FSIRX-B Data Input 0
FSITXA_D0	14			O	FSITX-A Data Output 0
FSIRXA_CLK	15			I	FSIRX-A Input Clock

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO10	0, 4, 8, 12	B2	1	I/O	General-Purpose Input Output 10
EPWM6A	1			O	ePWM-6 Output A (High-res available on ePWM1-8)
CANB_RX	2			I	CAN-B Receive
ADCSOCBO	3			O	ADC Start of Conversion B Output for External ADC (from ePWM modules)
EQEP1_A	5			I	eQEP-1 Input A
SCIB_TX	6			O	SCI-B Transmit Data
MCAN_RX	9			I	CAN/CAN-FD Receive
ESC_GPO2	10			O	EtherCAT General-Purpose Output 2
FSIRXB_D1	13			I	FSIRX-B Data Input 1
FSITXA_CLK	14			O	FSITX-A Output Clock
FSIRXA_D1	15			I	FSIRX-A Data Input 1
GPIO11	0, 4, 8, 12	C1	2	I/O	General-Purpose Input Output 11
EPWM6B	1			O	ePWM-6 Output B (High-res available on ePWM1-8)
SCIB_RX	2, 6			I	SCI-B Receive Data
OUTPUTXBAR7	3			O	Output X-BAR Output 7
EQEP1_B	5			I	eQEP-1 Input B
ESC_GPO3	10			O	EtherCAT General-Purpose Output 3
FSIRXB_CLK	13			I	FSIRX-B Input Clock
FSIRXA_D1	14			I	FSIRX-A Data Input 1
GPIO12	0, 4, 8, 12	C2	4	I/O	General-Purpose Input Output 12
EPWM7A	1			O	ePWM-7 Output A (High-res available on ePWM1-8)
CANB_TX	2			O	CAN-B Transmit
MDXB	3			O	McBSP-B Transmit Serial Data
EQEP1_STROBE	5			I/O	eQEP-1 Strobe
SCIC_TX	6			O	SCI-C Transmit Data
ESC_GPO4	10			O	EtherCAT General-Purpose Output 4
FSIRXC_D0	13			I	FSIRX-C Data Input 0
FSIRXA_D0	14			I	FSIRX-A Data Input 0
GPIO13	0, 4, 8, 12	D1	5	I/O	General-Purpose Input Output 13
EPWM7B	1			O	ePWM-7 Output B (High-res available on ePWM1-8)
CANB_RX	2			I	CAN-B Receive
MDRB	3			I	McBSP-B Receive Serial Data
EQEP1_INDEX	5			I/O	eQEP-1 Index
SCIC_RX	6			I	SCI-C Receive Data
ESC_GPO5	10			O	EtherCAT General-Purpose Output 5
FSIRXC_D1	13			I	FSIRX-C Data Input 1
FSIRXA_CLK	14			I	FSIRX-A Input Clock
GPIO14	0, 4, 8, 12	D2	6	I/O	General-Purpose Input Output 14
EPWM8A	1			O	ePWM-8 Output A (High-res available on ePWM1-8)
SCIB_TX	2			O	SCI-B Transmit Data
MCLKXB	3			O	McBSP-B Transmit Clock
OUTPUTXBAR3	6			O	Output X-BAR Output 3
ESC_GPO6	10			O	EtherCAT General-Purpose Output 6
FSIRXC_CLK	13			I	FSIRX-C Input Clock

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO15	0, 4, 8, 12	D3	7	I/O	General-Purpose Input Output 15
EPWM8B	1			O	ePWM-8 Output B (High-res available on ePWM1-8)
SCIB_RX	2			I	SCI-B Receive Data
MFSXB	3			O	McBSP-B Transmit Frame Sync
OUTPUTXBAR4	6			O	Output X-BAR Output 4
ESC_GPO7	10			O	EtherCAT General-Purpose Output 7
FSIRXD_D0	13			I	FSIRX-D Data Input 0
GPIO16	0, 4, 8, 12	E1	8	I/O	General-Purpose Input Output 16
SPIA_SIMO	1			I/O	SPI-A Slave In, Master Out (SIMO)
CANB_TX	2			O	CAN-B Transmit
OUTPUTXBAR7	3			O	Output X-BAR Output 7
EPWM9A	5			O	ePWM-9 Output A (High-res available on ePWM1-8)
SD1_D1	7			I	SDFM-1 Channel 1 Data Input
SSIA_TX	11			I/O	SSI-A Serial Data Transmit
FSIRXD_D1	13			I	FSIRX-D Data Input 1
GPIO17	0, 4, 8, 12	E2	9	I/O	General-Purpose Input Output 17
SPIA_SOMI	1			I/O	SPI-A Slave Out, Master In (SOMI)
CANB_RX	2			I	CAN-B Receive
OUTPUTXBAR8	3			O	Output X-BAR Output 8
EPWM9B	5			O	ePWM-9 Output B (High-res available on ePWM1-8)
SD1_C1	7			I	SDFM-1 Channel 1 Clock Input
SSIA_RX	11			I/O	SSI-A Serial Data Receive
FSIRXD_CLK	13			I	FSIRX-D Input Clock
GPIO18	0, 4, 8, 12	E3	10	I/O	General-Purpose Input Output 18
SPIA_CLK	1			I/O	SPI-A Clock
SCIB_TX	2			O	SCI-B Transmit Data
CANA_RX	3			I	CAN-A Receive
EPWM10A	5			O	ePWM-10 Output A (High-res available on ePWM1-8)
SD1_D2	7			I	SDFM-1 Channel 2 Data Input
MCAN_RX	9			I	CAN/CAN-FD Receive
EMIF1_CS2n	10			O	External memory interface 1 chip select 2
SSIA_CLK	11			I/O	SSI-A Clock
FSIRXE_D0	13			I	FSIRX-E Data Input 0
GPIO19	0, 4, 8, 12	E4	12	I/O	General-Purpose Input Output 19
SPIA_STEn	1			I/O	SPI-A Slave Transmit Enable (STE)
SCIB_RX	2			I	SCI-B Receive Data
CANA_TX	3			O	CAN-A Transmit
EPWM10B	5			O	ePWM-10 Output B (High-res available on ePWM1-8)
SD1_C2	7			I	SDFM-1 Channel 2 Clock Input
MCAN_TX	9			O	CAN/CAN-FD Transmit
EMIF1_CS3n	10			O	External memory interface 1 chip select 3
SSIA_FSS	11			I/O	SSI-A Frame Sync
FSIRXE_D1	13			I	FSIRX-E Data Input 1

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO20	0, 4, 8, 12	F2	13	I/O	General-Purpose Input Output 20
EQEP1_A	1			I	eQEP-1 Input A
MDXA	2			O	McBSP-A Transmit Serial Data
CANB_TX	3			O	CAN-B Transmit
EPWM11A	5			O	ePWM-11 Output A (High-res available on ePWM1-8)
SD1_D3	7			I	SDFM-1 Channel 3 Data Input
EMIF1_BA0	10			O	External memory interface 1 bank address 0
TRACE_DATA0	11			O	Trace Data 0
FSIRXE_CLK	13			I	FSIRX-E Input Clock
SPIC_SIMO	14			I/O	SPI-C Slave In, Master Out (SIMO)
GPIO21	0, 4, 8, 12	F3	14	I/O	General-Purpose Input Output 21
EQEP1_B	1			I	eQEP-1 Input B
MDRA	2			I	McBSP-A Receive Serial Data
CANB_RX	3			I	CAN-B Receive
EPWM11B	5			O	ePWM-11 Output B (High-res available on ePWM1-8)
SD1_C3	7			I	SDFM-1 Channel 3 Clock Input
EMIF1_BA1	10			O	External memory interface 1 bank address 1
TRACE_DATA1	11			O	Trace Data 1
FSIRXF_D0	13			I	FSIRX-F Data Input 0
SPIC_SOMI	14			I/O	SPI-C Slave Out, Master In (SOMI)
GPIO22	0, 4, 8, 12	J4	22	I/O	General-Purpose Input Output 22
EQEP1_STROBE	1			I/O	eQEP-1 Strobe
MCLKXA	2			O	McBSP-A Transmit Clock
SCIB_TX	3			O	SCI-B Transmit Data
EPWM12A	5			O	ePWM-12 Output A (High-res available on ePWM1-8)
SPIB_CLK	6			I/O	SPI-B Clock
SD1_D4	7			I	SDFM-1 Channel 4 Data Input
MCAN_TX	9			O	CAN/CAN-FD Transmit
EMIF1_RAS	10			O	External memory interface 1 row address strobe
TRACE_DATA2	11			O	Trace Data 2
FSIRXF_D1	13			I	FSIRX-F Data Input 1
SPIC_CLK	14			I/O	SPI-C Clock
GPIO23	0, 4, 8, 12	K4	23	I/O	General-Purpose Input Output 23
EQEP1_INDEX	1			I/O	eQEP-1 Index
MFSXA	2			O	McBSP-A Transmit Frame Sync
SCIB_RX	3			I	SCI-B Receive Data
EPWM12B	5			O	ePWM-12 Output B (High-res available on ePWM1-8)
SPIB_STEn	6			I/O	SPI-B Slave Transmit Enable (STE)
SD1_C4	7			I	SDFM-1 Channel 4 Clock Input
MCAN_RX	9			I	CAN/CAN-FD Receive
EMIF1_CAS	10			O	External memory interface 1 column address strobe
TRACE_DATA3	11			O	Trace Data 3
FSIRXF_CLK	13			I	FSIRX-F Input Clock
SPIC_STEn	14			I/O	SPI-C Slave Transmit Enable (STE)

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO24	0, 4, 8, 12	K3	24	I/O	General-Purpose Input Output 24
OUTPUTXBAR1	1			O	Output X-BAR Output 1
EQEP2_A	2			I	eQEP-2 Input A
MDXB	3			O	McBSP-B Transmit Serial Data
SPIB_SIMO	6			I/O	SPI-B Slave In, Master Out (SIMO)
SD2_D1	7			I	SDFM-2 Channel 1 Data Input
PMBUSA_SCL	9			I/OD	PMBus-A Open-Drain Bidirectional Clock
EMIF1_DQM0	10			O	External memory interface 1 Input/output mask for byte 0
TRACE_CLK	11			O	Trace Clock
EPWM13A	13			O	ePWM-13 Output A (High-res available on ePWM1-8)
FSIRXG_D0	15			I	FSIRX-G Data Input 0
GPIO25	0, 4, 8, 12	K2	25	I/O	General-Purpose Input Output 25
OUTPUTXBAR2	1			O	Output X-BAR Output 2
EQEP2_B	2			I	eQEP-2 Input B
MDRB	3			I	McBSP-B Receive Serial Data
SPIB_SOMI	6			I/O	SPI-B Slave Out, Master In (SOMI)
SD2_C1	7			I	SDFM-2 Channel 1 Clock Input
PMBUSA_SDA	9			I/OD	PMBus-A Open-Drain Bidirectional Data
EMIF1_DQM1	10			O	External memory interface 1 Input/output mask for byte 1
TRACE_SWO	11			O	Trace Single Wire Out
EPWM13B	13			O	ePWM-13 Output B (High-res available on ePWM1-8)
FSITXA_D1	14			O	FSITX-A Data Output 1
FSIRXG_D1	15			I	FSIRX-G Data Input 1
GPIO26	0, 4, 8, 12	K1	27	I/O	General-Purpose Input Output 26
OUTPUTXBAR3	1, 5			O	Output X-BAR Output 3
EQEP2_INDEX	2			I/O	eQEP-2 Index
MCLKXB	3			O	McBSP-B Transmit Clock
SPIB_CLK	6			I/O	SPI-B Clock
SD2_D2	7			I	SDFM-2 Channel 2 Data Input
PMBUSA_ALERT	9			I/OD	PMBus-A Open-Drain Bidirectional Alert Signal
EMIF1_DQM2	10			O	External memory interface 1 Input/output mask for byte 2
ESC_MDIO_CLK	11			O	EtherCAT MDIO Clock
EPWM14A	13			O	ePWM-14 Output A (High-res available on ePWM1-8)
FSITXA_D0	14			O	FSITX-A Data Output 0
FSIRXG_CLK	15			I	FSIRX-G Input Clock

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO27	0, 4, 8, 12	L1	28	I/O	General-Purpose Input Output 27
OUTPUTXBAR4	1, 5			O	Output X-BAR Output 4
EQEP2_STROBE	2			I/O	eQEP-2 Strobe
MFSXB	3			O	McBSP-B Transmit Frame Sync
SPIB_STEn	6			I/O	SPI-B Slave Transmit Enable (STE)
SD2_C2	7			I	SDFM-2 Channel 2 Clock Input
PMBUSA_CTL	9			I	PMBus-A Control Signal
EMIF1_DQM3	10			O	External memory interface 1 Input/output mask for byte 3
ESC_MDIO_DATA	11			I/O	EtherCAT MDIO Data
EPWM14B	13			O	ePWM-14 Output B (High-res available on ePWM1-8)
FSITXA_CLK	14			O	FSITX-A Output Clock
FSIRXH_D0	15			I	FSIRX-H Data Input 0
GPIO28	0, 4, 8, 12	V11	64	I/O	General-Purpose Input Output 28
SCIA_RX	1			I	SCI-A Receive Data
EMIF1_CS4n	2			O	External memory interface 1 chip select 4
OUTPUTXBAR5	5			O	Output X-BAR Output 5
EQEP3_A	6			I	eQEP-3 Input A
SD2_D3	7			I	SDFM-2 Channel 3 Data Input
EMIF1_CS2n	9			O	External memory interface 1 chip select 2
EPWM15A	13			O	ePWM-15 Output A (High-res available on ePWM1-8)
FSIRXH_D1	15			I	FSIRX-H Data Input 1
GPIO29	0, 4, 8, 12	W11	65	I/O	General-Purpose Input Output 29
SCIA_TX	1			O	SCI-A Transmit Data
EMIF1_SDCKE	2			O	External memory interface 1 SDRAM clock enable
OUTPUTXBAR6	5			O	Output X-BAR Output 6
EQEP3_B	6			I	eQEP-3 Input B
SD2_C3	7			I	SDFM-2 Channel 3 Clock Input
EMIF1_CS3n	9			O	External memory interface 1 chip select 3
ESC_LATCH0	10			I	EtherCAT LatchSignal Input 0
ESC_I2C_SDA	11			I/OC	EtherCAT I2C Data
EPWM15B	13			O	ePWM-15 Output B (High-res available on ePWM1-8)
ESC_SYNC0	14			O	EtherCAT SyncSignal Output 0
FSIRXH_CLK	15			I	FSIRX-H Input Clock
GPIO30	0, 4, 8, 12	T11	63	I/O	General-Purpose Input Output 30
CANA_RX	1			I	CAN-A Receive
EMIF1_CLK	2			O	External memory interface 1 clock
MCAN_RX	3			I	CAN/CAN-FD Receive
OUTPUTXBAR7	5			O	Output X-BAR Output 7
EQEP3_STROBE	6			I/O	eQEP-3 Strobe
SD2_D4	7			I	SDFM-2 Channel 4 Data Input
EMIF1_CS4n	9			O	External memory interface 1 chip select 4
ESC_LATCH1	10			I	EtherCAT LatchSignal Input 1
ESC_I2C_SCL	11			I/OC	EtherCAT I2C Clock
EPWM16A	13			O	ePWM-16 Output A (High-res available on ePWM1-8)
ESC_SYNC1	14			O	EtherCAT SyncSignal Output 1
SPID_SIMO	15			I/O	SPI-D Slave In, Master Out (SIMO)

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO31	0, 4, 8, 12	U11	66	I/O	General-Purpose Input Output 31
CANA_TX	1			O	CAN-A Transmit
EMIF1_WEn	2			O	External memory interface 1 write enable
MCAN_TX	3			O	CAN/CAN-FD Transmit
OUTPUTXBAR8	5			O	Output X-BAR Output 8
EQEP3_INDEX	6			I/O	eQEP-3 Index
SD2_C4	7			I	SDFM-2 Channel 4 Clock Input
EMIF1_RNW	9			O	External memory interface 1 read not write
I2CA_SDA	10			I/OD	I2C-A Open-Drain Bidirectional Data
CM-I2CA_SDA	11			I/OD	CM-I2C-A Open-Drain Bidirectional Data
EPWM16B	13			O	ePWM-16 Output B (High-res available on ePWM1-8)
SPID_SOMI	15			I/O	SPI-D Slave Out, Master In (SOMI)
GPIO32	0, 4, 8, 12	U13	67	I/O	General-Purpose Input Output 32
I2CA_SDA	1			I/OD	I2C-A Open-Drain Bidirectional Data
EMIF1_CS0n	2			O	External memory interface 1 chip select 0
SPIA_SIMO	3			I/O	SPI-A Slave In, Master Out (SIMO)
CLB_OUTPUTXBAR1	7			O	CLB Output X-BAR Output 1
EMIF1_OEn	9			O	External memory interface 1 output enable
I2CA_SCL	10			I/OD	I2C-A Open-Drain Bidirectional Clock
CM-I2CA_SCL	11			I/OD	CM-I2C-A Open-Drain Bidirectional Clock
SPID_CLK	15			I/O	SPI-D Clock
GPIO33	0, 4, 8, 12	T13	69	I/O	General-Purpose Input Output 33
I2CA_SCL	1			I/OD	I2C-A Open-Drain Bidirectional Clock
EMIF1_RNW	2			O	External memory interface 1 read not write
SPIA_SOMI	3			I/O	SPI-A Slave Out, Master In (SOMI)
CLB_OUTPUTXBAR2	7			O	CLB Output X-BAR Output 2
EMIF1_BA0	9			O	External memory interface 1 bank address 0
SPID_STEn	15			I/O	SPI-D Slave Transmit Enable (STE)
GPIO34	0, 4, 8, 12	U14	70	I/O	General-Purpose Input Output 34
OUTPUTXBAR1	1			O	Output X-BAR Output 1
EMIF1_CS2n	2			O	External memory interface 1 chip select 2
SPIA_CLK	3			I/O	SPI-A Clock
I2CB_SDA	6			I/OD	I2C-B Open-Drain Bidirectional Data
CLB_OUTPUTXBAR3	7			O	CLB Output X-BAR Output 3
EMIF1_BA1	9			O	External memory interface 1 bank address 1
ESC_LATCH0	10			I	EtherCAT LatchSignal Input 0
ENET_MII_CRS	11			I	EMAC MII carrier sense
SCIA_TX	13			O	SCI-A Transmit Data
ESC_SYNC0	14			O	EtherCAT SyncSignal Output 0

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO35	0, 4, 8, 12	T14	71	I/O	General-Purpose Input Output 35
SCIA_RX	1			I	SCI-A Receive Data
EMIF1_CS3n	2			O	External memory interface 1 chip select 3
SPIA_STEn	3			I/O	SPI-A Slave Transmit Enable (STE)
I2CB_SCL	6			I/OD	I2C-B Open-Drain Bidirectional Clock
CLB_OUTPUTXBAR4	7			O	CLB Output X-BAR Output 4
EMIF1_A0	9			O	External memory interface 1 address line 0
ESC_LATCH1	10			I	EtherCAT LatchSignal Input 1
ENET_MII_COL	11			I	EMAC MII collision detect
ESC_SYNC1	14			O	EtherCAT SyncSignal Output 1
GPIO36	0, 4, 8, 12	V16	83	I/O	General-Purpose Input Output 36
SCIA_TX	1			O	SCI-A Transmit Data
EMIF1_WAIT	2			I	External memory interface 1 Asynchronous SRAM WAIT
CANA_RX	6			I	CAN-A Receive
CLB_OUTPUTXBAR5	7			O	CLB Output X-BAR Output 5
EMIF1_A1	9			O	External memory interface 1 address line 1
MCAN_RX	10			I	CAN/CAN-FD Receive
SD1_D1	13			I	SDFM-1 Channel 1 Data Input
GPIO37	0, 4, 8, 12	U16	84	I/O	General-Purpose Input Output 37
OUTPUTXBAR2	1			O	Output X-BAR Output 2
EMIF1_OEn	2			O	External memory interface 1 output enable
CANA_TX	6			O	CAN-A Transmit
CLB_OUTPUTXBAR6	7			O	CLB Output X-BAR Output 6
EMIF1_A2	9			O	External memory interface 1 address line 2
MCAN_TX	10			O	CAN/CAN-FD Transmit
SD1_D2	13			I	SDFM-1 Channel 2 Data Input
GPIO38	0, 4, 8, 12	T16	85	I/O	General-Purpose Input Output 38
EMIF1_A0	2			O	External memory interface 1 address line 0
SCIC_TX	5			O	SCI-C Transmit Data
CANB_TX	6			O	CAN-B Transmit
CLB_OUTPUTXBAR7	7			O	CLB Output X-BAR Output 7
EMIF1_A3	9			O	External memory interface 1 address line 3
ENET_MII_RX_DV	10			I	EMAC MII receive data valid (or) RMII carrier sense/ receive data valid
ENET_MII_CRS	11			I	EMAC MII carrier sense
SD1_D3	13			I	SDFM-1 Channel 3 Data Input
GPIO39	0, 4, 8, 12	W17	86	I/O	General-Purpose Input Output 39
EMIF1_A1	2			O	External memory interface 1 address line 1
SCIC_RX	5			I	SCI-C Receive Data
CANB_RX	6			I	CAN-B Receive
CLB_OUTPUTXBAR8	7			O	CLB Output X-BAR Output 8
EMIF1_A4	9			O	External memory interface 1 address line 4
ENET_MII_RX_ERR	10			I	EMAC MII / RMII receive error
ENET_MII_COL	11			I	EMAC MII collision detect
SD1_D4	13			I	SDFM-1 Channel 4 Data Input

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO40	0, 4, 8, 12	V17	87	I/O	General-Purpose Input Output 40
EMIF1_A2	2			O	External memory interface 1 address line 2
I2CB_SDA	6			I/OD	I2C-B Open-Drain Bidirectional Data
ENET_MII_CRS	11			I	EMAC MII carrier sense
ESC_I2C_SDA	14			I/OC	EtherCAT I2C Data
GPIO41	0, 4, 8, 12	U17	89	I/O	General-Purpose Input Output 41
EMIF1_A3	2			O	External memory interface 1 address line 3
I2CB_SCL	6			I/OD	I2C-B Open-Drain Bidirectional Clock
ENET_REVMII_MDIO_RST	10			I	EMAC REVMII MDIO reset
ENET_MII_COL	11			I	EMAC MII collision detect
ESC_I2C_SCL	14			I/OC	EtherCAT I2C Clock
GPIO42	0, 4, 8, 12	D19	130	I/O	General-Purpose Input Output 42
I2CA_SDA	6			I/OD	I2C-A Open-Drain Bidirectional Data
ENET_MDIO_CLK	10			I/O	EMAC management data clock, Output in MII/RMII modes, Input in RevMII mode
UARTA_TX	11			I/O	UART-A Serial Data Transmit
SCIA_TX	15			O	SCI-A Transmit Data
USB0DM	ALT			O	USB-0 PHY differential data
GPIO43	0, 4, 8, 12	C19	131	I/O	General-Purpose Input Output 43
I2CA_SCL	6			I/OD	I2C-A Open-Drain Bidirectional Clock
ENET_MDIO_DATA	10			I/O	EMAC management data
UARTA_RX	11			I/O	UART-A Serial Data Receive
SCIA_RX	15			I	SCI-A Receive Data
USB0DP	ALT			O	USB-0 PHY differential data
GPIO44	0, 4, 8, 12	K18	113	I/O	General-Purpose Input Output 44
EMIF1_A4	2			O	External memory interface 1 address line 4
ENET_MII_TX_CLK	11			I	EMAC MII transmit clock
ESC_TX1_CLK	14			I	EtherCAT MII Transmit-1 Clock
GPIO45	0, 4, 8, 12	K19	115	I/O	General-Purpose Input Output 45
EMIF1_A5	2			O	External memory interface 1 address line 5
ENET_MII_TX_EN	11			O	EMAC MII / RMII transmit enable
ESC_TX1_ENA	14			I/O	EtherCAT MII Transmit-1 Enable
GPIO46	0, 4, 8, 12	E19	128	I/O	General-Purpose Input Output 46
EMIF1_A6	2			O	External memory interface 1 address line 6
SCID_RX	6			I	SCI-D Receive Data
ENET_MII_TX_ERR	11			O	EMAC MII transmit error
ESC_MDIO_CLK	14			O	EtherCAT MDIO Clock
GPIO47	0, 4, 8, 12	E18	129	I/O	General-Purpose Input Output 47
EMIF1_A7	2			O	External memory interface 1 address line 7
SCID_TX	6			O	SCI-D Transmit Data
ENET_PPS0	11			O	EMAC Pulse Per Second Output 0
ESC_MDIO_DATA	14			I/O	EtherCAT MDIO Data

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO48	0, 4, 8, 12			I/O	General-Purpose Input Output 48
OUTPUTXBAR3	1			O	Output X-BAR Output 3
EMIF1_A8	2			O	External memory interface 1 address line 8
SCIA_TX	6	R16	90	O	SCI-A Transmit Data
SD1_D1	7			I	SDFM-1 Channel 1 Data Input
ENET_PPS1	11			O	EMAC Pulse Per Second Output 1
ESC_PHY_CLK	14			O	EtherCAT PHY Clock
GPIO49	0, 4, 8, 12			I/O	General-Purpose Input Output 49
OUTPUTXBAR4	1			O	Output X-BAR Output 4
EMIF1_A9	2			O	External memory interface 1 address line 9
SCIA_RX	6			I	SCI-A Receive Data
SD1_C1	7	R17	93	I	SDFM-1 Channel 1 Clock Input
EMIF1_A5	9			O	External memory interface 1 address line 5
ENET_MII_RX_CLK	11			I	EMAC MII receive clock
SD2_D1	13			I	SDFM-2 Channel 1 Data Input
FSITXA_D0	14			O	FSITX-A Data Output 0
GPIO50	0, 4, 8, 12			I/O	General-Purpose Input Output 50
EQEP1_A	1			I	eQEP-1 Input A
EMIF1_A10	2			O	External memory interface 1 address line 10
SPIC_SIMO	6			I/O	SPI-C Slave In, Master Out (SIMO)
SD1_D2	7	R18	94	I	SDFM-1 Channel 2 Data Input
EMIF1_A6	9			O	External memory interface 1 address line 6
ENET_MII_RX_DV	11			I	EMAC MII receive data valid (or) RMII carrier sense/ receive data valid
SD2_D2	13			I	SDFM-2 Channel 2 Data Input
FSITXA_D1	14			O	FSITX-A Data Output 1
GPIO51	0, 4, 8, 12			I/O	General-Purpose Input Output 51
EQEP1_B	1			I	eQEP-1 Input B
EMIF1_A11	2			O	External memory interface 1 address line 11
SPIC_SOMI	6			I/O	SPI-C Slave Out, Master In (SOMI)
SD1_C2	7	R19	95	I	SDFM-1 Channel 2 Clock Input
EMIF1_A7	9			O	External memory interface 1 address line 7
ENET_MII_RX_ERR	11			I	EMAC MII / RMII receive error
SD2_D3	13			I	SDFM-2 Channel 3 Data Input
FSITXA_CLK	14			O	FSITX-A Output Clock
GPIO52	0, 4, 8, 12			I/O	General-Purpose Input Output 52
EQEP1_STROBE	1			I/O	eQEP-1 Strobe
EMIF1_A12	2			O	External memory interface 1 address line 12
SPIC_CLK	6			I/O	SPI-C Clock
SD1_D3	7	P16	96	I	SDFM-1 Channel 3 Data Input
EMIF1_A8	9			O	External memory interface 1 address line 8
ENET_MII_RX_DATA0	11			I	EMAC MII / RMII receive data 0
SD2_D4	13			I	SDFM-2 Channel 4 Data Input
FSIRXA_D0	14			I	FSIRX-A Data Input 0

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO53	0, 4, 8, 12	P17	97	I/O	General-Purpose Input Output 53
EQEP1_INDEX	1			I/O	eQEP-1 Index
EMIF1_D31	2			I/O	External memory interface 1 data line 31
EMIF2_D15	3			I/O	External memory interface 2 data line 15
SPIC_STEn	6			I/O	SPI-C Slave Transmit Enable (STE)
SD1_C3	7			I	SDFM-1 Channel 3 Clock Input
EMIF1_A9	9			O	External memory interface 1 address line 9
ENET_MII_RX_DATA1	11			I	EMAC MII / RMII receive data 1
SD1_C1	13			I	SDFM-1 Channel 1 Clock Input
FSIRXA_D1	14			I	FSIRX-A Data Input 1
GPIO54	0, 4, 8, 12	P18	98	I/O	General-Purpose Input Output 54
SPIA_SIMO	1			I/O	SPI-A Slave In, Master Out (SIMO)
EMIF1_D30	2			I/O	External memory interface 1 data line 30
EMIF2_D14	3			I/O	External memory interface 2 data line 14
EQEP2_A	5			I	eQEP-2 Input A
SCIB_TX	6			O	SCI-B Transmit Data
SD1_D4	7			I	SDFM-1 Channel 4 Data Input
EMIF1_A10	9			O	External memory interface 1 address line 10
ENET_MII_RX_DATA2	11			I	EMAC MII receive data 2
SD1_C2	13			I	SDFM-1 Channel 2 Clock Input
FSIRXA_CLK	14			I	FSIRX-A Input Clock
SSIA_TX	15			I/O	SSI-A Serial Data Transmit
GPIO55	0, 4, 8, 12	P19	100	I/O	General-Purpose Input Output 55
SPIA_SOMI	1			I/O	SPI-A Slave Out, Master In (SOMI)
EMIF1_D29	2			I/O	External memory interface 1 data line 29
EMIF2_D13	3			I/O	External memory interface 2 data line 13
EQEP2_B	5			I	eQEP-2 Input B
SCIB_RX	6			I	SCI-B Receive Data
SD1_C4	7			I	SDFM-1 Channel 4 Clock Input
EMIF1_D0	9			I/O	External memory interface 1 data line 0
ENET_MII_RX_DATA3	11			I	EMAC MII receive data 3
SD1_C3	13			I	SDFM-1 Channel 3 Clock Input
FSITXB_D0	14			O	FSITX-B Data Output 0
SSIA_RX	15			I/O	SSI-A Serial Data Receive

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO56	0, 4, 8, 12	N16	101	I/O	General-Purpose Input Output 56
SPIA_CLK	1			I/O	SPI-A Clock
EMIF1_D28	2			I/O	External memory interface 1 data line 28
EMIF2_D12	3			I/O	External memory interface 2 data line 12
EQEP2_STROBE	5			I/O	eQEP-2 Strobe
SCIC_TX	6			O	SCI-C Transmit Data
SD2_D1	7			I	SDFM-2 Channel 1 Data Input
EMIF1_D1	9			I/O	External memory interface 1 data line 1
I2CA_SDA	10			I/OD	I2C-A Open-Drain Bidirectional Data
ENET_MII_TX_EN	11			O	EMAC MII / RMII transmit enable
SD1_C4	13			I	SDFM-1 Channel 4 Clock Input
FSITXB_CLK	14			O	FSITX-B Output Clock
SSIA_CLK	15			I/O	SSI-A Clock
GPIO57	0, 4, 8, 12	N18	102	I/O	General-Purpose Input Output 57
SPIA_STEn	1			I/O	SPI-A Slave Transmit Enable (STE)
EMIF1_D27	2			I/O	External memory interface 1 data line 27
EMIF2_D11	3			I/O	External memory interface 2 data line 11
EQEP2_INDEX	5			I/O	eQEP-2 Index
SCIC_RX	6			I	SCI-C Receive Data
SD2_C1	7			I	SDFM-2 Channel 1 Clock Input
EMIF1_D2	9			I/O	External memory interface 1 data line 2
I2CA_SCL	10			I/OD	I2C-A Open-Drain Bidirectional Clock
ENET_MII_TX_ERR	11			O	EMAC MII transmit error
FSITXB_D1	14			O	FSITX-B Data Output 1
SSIA_FSS	15			I/O	SSI-A Frame Sync
GPIO58	0, 4, 8, 12	N17	103	I/O	General-Purpose Input Output 58
MCLKRA	1			I	McBSP-A Receive Clock
EMIF1_D26	2			I/O	External memory interface 1 data line 26
EMIF2_D10	3			I/O	External memory interface 2 data line 10
OUTPUTXBAR1	5			O	Output X-BAR Output 1
SPIB_CLK	6			I/O	SPI-B Clock
SD2_D2	7			I	SDFM-2 Channel 2 Data Input
EMIF1_D3	9			I/O	External memory interface 1 data line 3
ESC_LED_LINK0_ACTIVE	10			O	EtherCAT Link-0 Active
ENET_MII_TX_CLK	11			I	EMAC MII transmit clock
SD2_C2	13			I	SDFM-2 Channel 2 Clock Input
FSIRXB_D0	14			I	FSIRX-B Data Input 0
SPIA_SIMO	15			I/O	SPI-A Slave In, Master Out (SIMO)

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO59	0, 4, 8, 12			I/O	General-Purpose Input Output 59
MFSRA	1			I	McBSP-A Receive Frame Sync
EMIF1_D25	2			I/O	External memory interface 1 data line 25
EMIF2_D9	3			I/O	External memory interface 2 data line 9
OUTPUTXBAR2	5			O	Output X-BAR Output 2
SPIB_STEn	6			I/O	SPI-B Slave Transmit Enable (STE)
SD2_C2	7	M16	104	I	SDFM-2 Channel 2 Clock Input
EMIF1_D4	9			I/O	External memory interface 1 data line 4
ESC_LED_LINK1_ACTIVE	10			O	EtherCAT Link-1 Active
ENET_MII_TX_DATA0	11			O	EMAC MII / RMII transmit data 0
SD2_C3	13			I	SDFM-2 Channel 3 Clock Input
FSIRXB_D1	14			I	FSIRX-B Data Input 1
SPIA_SOMI	15			I/O	SPI-A Slave Out, Master In (SOMI)
GPIO60	0, 4, 8, 12			I/O	General-Purpose Input Output 60
MCLKRB	1			I	McBSP-B Receive Clock
EMIF1_D24	2			I/O	External memory interface 1 data line 24
EMIF2_D8	3			I/O	External memory interface 2 data line 8
OUTPUTXBAR3	5			O	Output X-BAR Output 3
SPIB_SIMO	6			I/O	SPI-B Slave In, Master Out (SIMO)
SD2_D3	7	M17	105	I	SDFM-2 Channel 3 Data Input
EMIF1_D5	9			I/O	External memory interface 1 data line 5
ESC_LED_ERR	10			O	EtherCAT Error LED
ENET_MII_TX_DATA1	11			O	EMAC MII / RMII transmit data 1
SD2_C4	13			I	SDFM-2 Channel 4 Clock Input
FSIRXB_CLK	14			I	FSIRX-B Input Clock
SPIA_CLK	15			I/O	SPI-A Clock
GPIO61	0, 4, 8, 12			I/O	General-Purpose Input Output 61
MFSRB	1			I	McBSP-B Receive Frame Sync
EMIF1_D23	2			I/O	External memory interface 1 data line 23
EMIF2_D7	3			I/O	External memory interface 2 data line 7
OUTPUTXBAR4	5			O	Output X-BAR Output 4
SPIB_SOMI	6	L16	107	I/O	SPI-B Slave Out, Master In (SOMI)
SD2_C3	7			I	SDFM-2 Channel 3 Clock Input
EMIF1_D6	9			I/O	External memory interface 1 data line 6
ESC_LED_RUN	10			O	EtherCAT Run LED
ENET_MII_TX_DATA2	11			O	EMAC MII transmit data 2
CANA_RX	14			I	CAN-A Receive
SPIA_STEn	15			I/O	SPI-A Slave Transmit Enable (STE)

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO62	0, 4, 8, 12	J17	108	I/O	General-Purpose Input Output 62
SCIC_RX	1			I	SCI-C Receive Data
EMIF1_D22	2			I/O	External memory interface 1 data line 22
EMIF2_D6	3			I/O	External memory interface 2 data line 6
EQEP3_A	5			I	eQEP-3 Input A
CANA_RX	6			I	CAN-A Receive
SD2_D4	7			I	SDFM-2 Channel 4 Data Input
EMIF1_D7	9			I/O	External memory interface 1 data line 7
ESC_LED_STATE_RUN	10			O	EtherCAT State Run
ENET_MII_TX_DATA3	11			O	EMAC MII transmit data 3
CANA_TX	14			O	CAN-A Transmit
GPIO63	0, 4, 8, 12	J16	109	I/O	General-Purpose Input Output 63
SCIC_TX	1			O	SCI-C Transmit Data
EMIF1_D21	2			I/O	External memory interface 1 data line 21
EMIF2_D5	3			I/O	External memory interface 2 data line 5
EQEP3_B	5			I	eQEP-3 Input B
CANA_TX	6			O	CAN-A Transmit
SD2_C4	7			I	SDFM-2 Channel 4 Clock Input
SSIA_TX	9			I/O	SSI-A Serial Data Transmit
ENET_MII_RX_DATA0	11			I	EMAC MII / RMII receive data 0
SD1_D1	13			I	SDFM-1 Channel 1 Data Input
ESC_RX1_DATA0	14			I	EtherCAT MII Receive-1 Data-0
SPIB_SIMO	15			I/O	SPI-B Slave In, Master Out (SIMO)
GPIO64	0, 4, 8, 12	L17	110	I/O	General-Purpose Input Output 64
EMIF1_D20	2			I/O	External memory interface 1 data line 20
EMIF2_D4	3			I/O	External memory interface 2 data line 4
EQEP3_STROBE	5			I/O	eQEP-3 Strobe
SCIA_RX	6			I	SCI-A Receive Data
SSIA_RX	9			I/O	SSI-A Serial Data Receive
ENET_MII_RX_DV	10			I	EMAC MII receive data valid (or) RMII carrier sense/ receive data valid
ENET_MII_RX_DATA1	11			I	EMAC MII / RMII receive data 1
SD1_C1	13			I	SDFM-1 Channel 1 Clock Input
ESC_RX1_DATA1	14			I	EtherCAT MII Receive-1 Data-1
SPIB_SOMI	15			I/O	SPI-B Slave Out, Master In (SOMI)
GPIO65	0, 4, 8, 12	K16	111	I/O	General-Purpose Input Output 65
EMIF1_D19	2			I/O	External memory interface 1 data line 19
EMIF2_D3	3			I/O	External memory interface 2 data line 3
EQEP3_INDEX	5			I/O	eQEP-3 Index
SCIA_TX	6			O	SCI-A Transmit Data
SSIA_CLK	9			I/O	SSI-A Clock
ENET_MII_RX_ERR	10			I	EMAC MII / RMII receive error
ENET_MII_RX_DATA2	11			I	EMAC MII receive data 2
SD1_D2	13			I	SDFM-1 Channel 2 Data Input
ESC_RX1_DATA2	14			I	EtherCAT MII Receive-1 Data-2
SPIB_CLK	15			I/O	SPI-B Clock

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO66	0, 4, 8, 12	K17	112	I/O	General-Purpose Input Output 66
EMIF1_D18	2			I/O	External memory interface 1 data line 18
EMIF2_D2	3			I/O	External memory interface 2 data line 2
I2CB_SDA	6			I/OD	I2C-B Open-Drain Bidirectional Data
SSIA_FSS	9			I/O	SSI-A Frame Sync
ENET_MII_RX_DATA0	10			I	EMAC MII / RMII receive data 0
ENET_MII_RX_DATA3	11			I	EMAC MII receive data 3
SD1_C2	13			I	SDFM-1 Channel 2 Clock Input
ESC_RX1_DATA3	14			I	EtherCAT MII Receive-1 Data-3
SPIB_STEn	15			I/O	SPI-B Slave Transmit Enable (STE)
GPIO67	0, 4, 8, 12	B19	132	I/O	General-Purpose Input Output 67
EMIF1_D17	2			I/O	External memory interface 1 data line 17
EMIF2_D1	3			I/O	External memory interface 2 data line 1
ENET_MII_RX_CLK	10			I	EMAC MII receive clock
ENET_REVMII_MDIO_RST	11			I	EMAC REVMII MDIO reset
SD1_D3	13			I	SDFM-1 Channel 3 Data Input
GPIO68	0, 4, 8, 12	C18	133	I/O	General-Purpose Input Output 68
EMIF1_D16	2			I/O	External memory interface 1 data line 16
EMIF2_D0	3			I/O	External memory interface 2 data line 0
ENET_MII_INTR	11			I/O	EMAC PHY interrupt, Input in MII/RMII mode, Output in RevMII mode
SD1_C3	13			I	SDFM-1 Channel 3 Clock Input
ESC_PHY1_LINKSTATUS	14			I	EtherCAT PHY-1 Link Status
GPIO69	0, 4, 8, 12	B18	134	I/O	General-Purpose Input Output 69
EMIF1_D15	2			I/O	External memory interface 1 data line 15
I2CB_SCL	6			I/OD	I2C-B Open-Drain Bidirectional Clock
ENET_MII_TX_EN	10			O	EMAC MII / RMII transmit enable
ENET_MII_RX_CLK	11			I	EMAC MII receive clock
SD1_D4	13			I	SDFM-1 Channel 4 Data Input
ESC_RX1_CLK	14			I	EtherCAT MII Receive-1 Clock
SPIC_SIMO	15			I/O	SPI-C Slave In, Master Out (SIMO)
GPIO70	0, 4, 8, 12	A17	135	I/O	General-Purpose Input Output 70
EMIF1_D14	2			I/O	External memory interface 1 data line 14
CANA_RX	5			I	CAN-A Receive
SCIB_TX	6			O	SCI-B Transmit Data
MCAN_RX	9			I	CAN/CAN-FD Receive
ENET_MII_RX_DV	11			I	EMAC MII receive data valid (or) RMII carrier sense/ receive data valid
SD1_C4	13			I	SDFM-1 Channel 4 Clock Input
ESC_RX1_DV	14			I	EtherCAT MII Receive-1 Data Valid
SPIC_SOMI	15			I/O	SPI-C Slave Out, Master In (SOMI)

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO71	0, 4, 8, 12	B17	136	I/O	General-Purpose Input Output 71
EMIF1_D13	2			I/O	External memory interface 1 data line 13
CANA_TX	5			O	CAN-A Transmit
SCIB_RX	6			I	SCI-B Receive Data
MCAN_TX	9			O	CAN/CAN-FD Transmit
ENET_MII_RX_DATA0	10			I	EMAC MII / RMII receive data 0
ENET_MII_RX_ERR	11			I	EMAC MII / RMII receive error
ESC_RX1_ERR	14			I	EtherCAT MII Receive-1 Error
SPIC_CLK	15			I/O	SPI-C Clock
GPIO72	0, 4, 8, 12	B16	139	I/O	General-Purpose Input Output 72
EMIF1_D12	2			I/O	External memory interface 1 data line 12
CANB_TX	5			O	CAN-B Transmit
SCIC_TX	6			O	SCI-C Transmit Data
ENET_MII_RX_DATA1	10			I	EMAC MII / RMII receive data 1
ENET_MII_TX_DATA3	11			O	EMAC MII transmit data 3
ESC_TX1_DATA3	14			O	EtherCAT MII Transmit-1 Data-3
SPIC_STEn	15			I/O	SPI-C Slave Transmit Enable (STE)
GPIO73	0, 4, 8, 12	A16	140	I/O	General-Purpose Input Output 73
EMIF1_D11	2			I/O	External memory interface 1 data line 11
XCLKOUT	3			O	External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device.
CANB_RX	5			I	CAN-B Receive
SCIC_RX	6			I	SCI-C Receive Data
ENET_RMII_CLK	10			I/O	EMAC RMII clock
ENET_MII_TX_DATA2	11			O	EMAC MII transmit data 2
SD2_D2	13			I	SDFM-2 Channel 2 Data Input
ESC_TX1_DATA2	14			O	EtherCAT MII Transmit-1 Data-2
GPIO74	0, 4, 8, 12	C17	141	I/O	General-Purpose Input Output 74
EMIF1_D10	2			I/O	External memory interface 1 data line 10
MCAN_TX	9			O	CAN/CAN-FD Transmit
ENET_MII_TX_DATA1	11			O	EMAC MII / RMII transmit data 1
SD2_C2	13			I	SDFM-2 Channel 2 Clock Input
ESC_TX1_DATA1	14			O	EtherCAT MII Transmit-1 Data-1
GPIO75	0, 4, 8, 12	D16	142	I/O	General-Purpose Input Output 75
EMIF1_D9	2			I/O	External memory interface 1 data line 9
MCAN_RX	9			I	CAN/CAN-FD Receive
ENET_MII_TX_DATA0	11			O	EMAC MII / RMII transmit data 0
SD2_D3	13			I	SDFM-2 Channel 3 Data Input
ESC_TX1_DATA0	14			O	EtherCAT MII Transmit-1 Data-0
GPIO76	0, 4, 8, 12	C16	143	I/O	General-Purpose Input Output 76
EMIF1_D8	2			I/O	External memory interface 1 data line 8
SCID_TX	6			O	SCI-D Transmit Data
ENET_MII_RX_ERR	10			I	EMAC MII / RMII receive error
SD2_C3	13			I	SDFM-2 Channel 3 Clock Input
ESC_PHY_RESETn	14			O	EtherCAT PHY Active Low Reset

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO77	0, 4, 8, 12			I/O	General-Purpose Input Output 77
EMIF1_D7	2			I/O	External memory interface 1 data line 7
SCID_RX	6	A15	144	I	SCI-D Receive Data
SD2_D4	13			I	SDFM-2 Channel 4 Data Input
ESC_RX0_CLK	14			I	EtherCAT MII Receive-0 Clock
GPIO78	0, 4, 8, 12			I/O	General-Purpose Input Output 78
EMIF1_D6	2			I/O	External memory interface 1 data line 6
EQEP2_A	6	B15	145	I	eQEP-2 Input A
SD2_C4	13			I	SDFM-2 Channel 4 Clock Input
ESC_RX0_DV	14			I	EtherCAT MII Receive-0 Data Valid
GPIO79	0, 4, 8, 12			I/O	General-Purpose Input Output 79
EMIF1_D5	2			I/O	External memory interface 1 data line 5
EQEP2_B	6	C15	146	I	eQEP-2 Input B
SD2_D1	13			I	SDFM-2 Channel 1 Data Input
ESC_RX0_ERR	14			I	EtherCAT MII Receive-0 Error
GPIO80	0, 4, 8, 12			I/O	General-Purpose Input Output 80
EMIF1_D4	2			I/O	External memory interface 1 data line 4
EQEP2_STROBE	6	D15	148	I/O	eQEP-2 Strobe
SD2_C1	13			I	SDFM-2 Channel 1 Clock Input
ESC_RX0_DATA0	14			I	EtherCAT MII Receive-0 Data-0
GPIO81	0, 4, 8, 12			I/O	General-Purpose Input Output 81
EMIF1_D3	2	A14	149	I/O	External memory interface 1 data line 3
EQEP2_INDEX	6			I/O	eQEP-2 Index
ESC_RX0_DATA1	14			I	EtherCAT MII Receive-0 Data-1
GPIO82	0, 4, 8, 12			I/O	General-Purpose Input Output 82
EMIF1_D2	2	B14	150	I/O	External memory interface 1 data line 2
ESC_RX0_DATA2	14			I	EtherCAT MII Receive-0 Data-2
GPIO83	0, 4, 8, 12			I/O	General-Purpose Input Output 83
EMIF1_D1	2	C14	151	I/O	External memory interface 1 data line 1
ESC_RX0_DATA3	14			I	EtherCAT MII Receive-0 Data-3
GPIO84	0, 4, 8, 12			I/O	General-Purpose Input Output 84
SCIA_TX	5			O	SCI-A Transmit Data
MDXB	6	A11	154	O	McBSP-B Transmit Serial Data
UARTA_TX	11			I/O	UART-A Serial Data Transmit
ESC_TX0_ENA	14			I/O	EtherCAT MII Transmit-0 Enable
MDXA	15			O	McBSP-A Transmit Serial Data
GPIO85	0, 4, 8, 12			I/O	General-Purpose Input Output 85
EMIF1_D0	2			I/O	External memory interface 1 data line 0
SCIA_RX	5			I	SCI-A Receive Data
MDRB	6	B11	155	I	McBSP-B Receive Serial Data
UARTA_RX	11			I/O	UART-A Serial Data Receive
ESC_TX0_CLK	14			I	EtherCAT MII Transmit-0 Clock
MDRA	15			I	McBSP-A Receive Serial Data

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO86	0, 4, 8, 12	C11	156	I/O	General-Purpose Input Output 86
EMIF1_A13	2			O	External memory interface 1 address line 13
EMIF1_CAS	3			O	External memory interface 1 column address strobe
SCIB_TX	5			O	SCI-B Transmit Data
MCLKXB	6			O	McBSP-B Transmit Clock
ESC_PHY0_LINKSTATUS	14			I	EtherCAT PHY-0 Link Status
MCLKXA	15			O	McBSP-A Transmit Clock
GPIO87	0, 4, 8, 12	D11	157	I/O	General-Purpose Input Output 87
EMIF1_A14	2			O	External memory interface 1 address line 14
EMIF1_RAS	3			O	External memory interface 1 row address strobe
SCIB_RX	5			I	SCI-B Receive Data
MFSXB	6			O	McBSP-B Transmit Frame Sync
EMIF1_DQM3	9			O	External memory interface 1 Input/output mask for byte 3
ESC_TX0_DATA0	14			O	EtherCAT MII Transmit-0 Data-0
MFSXA	15			O	McBSP-A Transmit Frame Sync
GPIO88	0, 4, 8, 12	C6	170	I/O	General-Purpose Input Output 88
EMIF1_A15	2			O	External memory interface 1 address line 15
EMIF1_DQM0	3			O	External memory interface 1 Input/output mask for byte 0
EMIF1_DQM1	9			O	External memory interface 1 Input/output mask for byte 1
ESC_TX0_DATA1	14			O	EtherCAT MII Transmit-0 Data-1
GPIO89	0, 4, 8, 12	D6	171	I/O	General-Purpose Input Output 89
EMIF1_A16	2			O	External memory interface 1 address line 16
EMIF1_DQM1	3			O	External memory interface 1 Input/output mask for byte 1
SCIC_TX	6			O	SCI-C Transmit Data
EMIF1_CAS	9			O	External memory interface 1 column address strobe
ESC_TX0_DATA2	14			O	EtherCAT MII Transmit-0 Data-2
GPIO90	0, 4, 8, 12	A5	172	I/O	General-Purpose Input Output 90
EMIF1_A17	2			O	External memory interface 1 address line 17
EMIF1_DQM2	3			O	External memory interface 1 Input/output mask for byte 2
SCIC_RX	6			I	SCI-C Receive Data
EMIF1_RAS	9			O	External memory interface 1 row address strobe
ESC_TX0_DATA3	14			O	EtherCAT MII Transmit-0 Data-3
GPIO91	0, 4, 8, 12	B5	173	I/O	General-Purpose Input Output 91
EMIF1_A18	2			O	External memory interface 1 address line 18
EMIF1_DQM3	3			O	External memory interface 1 Input/output mask for byte 3
I2CA_SDA	6			I/OD	I2C-A Open-Drain Bidirectional Data
EMIF1_DQM2	9			O	External memory interface 1 Input/output mask for byte 2
PMBUSA_SCL	10			I/OD	PMBus-A Open-Drain Bidirectional Clock
SSIA_TX	11			I/O	SSI-A Serial Data Transmit
FSIRXF_D0	13			I	FSIRX-F Data Input 0
CLB_OUTPUTXBAR1	14			O	CLB Output X-BAR Output 1
SPID_SIMO	15			I/O	SPI-D Slave In, Master Out (SIMO)

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO92	0, 4, 8, 12	A4	174	I/O	General-Purpose Input Output 92
EMIF1_A19	2			O	External memory interface 1 address line 19
EMIF1_BA1	3			O	External memory interface 1 bank address 1
I2CA_SCL	6			I/OD	I2C-A Open-Drain Bidirectional Clock
EMIF1_DQM0	9			O	External memory interface 1 Input/output mask for byte 0
PMBUSA_SDA	10			I/OD	PMBus-A Open-Drain Bidirectional Data
SSIA_RX	11			I/O	SSI-A Serial Data Receive
FSIRXF_D1	13			I	FSIRX-F Data Input 1
CLB_OUTPUTXBAR2	14			O	CLB Output X-BAR Output 2
SPID_SOMI	15			I/O	SPI-D Slave Out, Master In (SOMI)
GPIO93	0, 4, 8, 12	B4	175	I/O	General-Purpose Input Output 93
EMIF1_BA0	3			O	External memory interface 1 bank address 0
SCID_TX	6			O	SCI-D Transmit Data
PMBUSA_ALERT	10			I/OD	PMBus-A Open-Drain Bidirectional Alert Signal
SSIA_CLK	11			I/O	SSI-A Clock
FSIRXF_CLK	13			I	FSIRX-F Input Clock
CLB_OUTPUTXBAR3	14			O	CLB Output X-BAR Output 3
SPID_CLK	15			I/O	SPI-D Clock
GPIO94	0, 4, 8, 12	A3	176	I/O	General-Purpose Input Output 94
SCID_RX	6			I	SCI-D Receive Data
EMIF1_BA1	9			O	External memory interface 1 bank address 1
PMBUSA_CTL	10			I	PMBus-A Control Signal
SSIA_FSS	11			I/O	SSI-A Frame Sync
FSIRXG_D0	13			I	FSIRX-G Data Input 0
CLB_OUTPUTXBAR4	14			O	CLB Output X-BAR Output 4
SPID_STEn	15			I/O	SPI-D Slave Transmit Enable (STE)
GPIO95	0, 4, 8, 12	B3		I/O	General-Purpose Input Output 95
EMIF2_A12	3			O	External memory interface 2 address line 12
FSIRXG_D1	13			I	FSIRX-G Data Input 1
CLB_OUTPUTXBAR5	14			O	CLB Output X-BAR Output 5
GPIO96	0, 4, 8, 12	C3		I/O	General-Purpose Input Output 96
EMIF2_DQM1	3			O	External memory interface 2 Input/output mask for byte 1
EQEP1_A	5			I	eQEP-1 Input A
FSIRXG_CLK	13			I	FSIRX-G Input Clock
CLB_OUTPUTXBAR6	14			O	CLB Output X-BAR Output 6
GPIO97	0, 4, 8, 12	A2		I/O	General-Purpose Input Output 97
EMIF2_DQM0	3			O	External memory interface 2 Input/output mask for byte 0
EQEP1_B	5			I	eQEP-1 Input B
FSIRXH_D0	13			I	FSIRX-H Data Input 0
CLB_OUTPUTXBAR7	14			O	CLB Output X-BAR Output 7
GPIO98	0, 4, 8, 12	F1		I/O	General-Purpose Input Output 98
EMIF2_A0	3			O	External memory interface 2 address line 0
EQEP1_STROBE	5			I/O	eQEP-1 Strobe
FSIRXH_D1	13			I	FSIRX-H Data Input 1
CLB_OUTPUTXBAR8	14			O	CLB Output X-BAR Output 8

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO99	0, 4, 8, 12	G1	17	I/O	General-Purpose Input Output 99
EMIF2_A1	3			O	External memory interface 2 address line 1
EQEP1_INDEX	5			I/O	eQEP-1 Index
FSIRXH_CLK	13			I	FSIRX-H Input Clock
GPIO100	0, 4, 8, 12	H1		I/O	General-Purpose Input Output 100
EMIF2_A2	3			O	External memory interface 2 address line 2
EQEP2_A	5			I	eQEP-2 Input A
SPIC_SIMO	6			I/O	SPI-C Slave In, Master Out (SIMO)
ESC_GPI0	10			I	EtherCAT General-Purpose Input 0
FSITXA_D0	13			O	FSITX-A Data Output 0
GPIO101	0, 4, 8, 12	H2		I/O	General-Purpose Input Output 101
EMIF2_A3	3			O	External memory interface 2 address line 3
EQEP2_B	5			I	eQEP-2 Input B
SPIC_SOMI	6			I/O	SPI-C Slave Out, Master In (SOMI)
ESC_GPI1	10			I	EtherCAT General-Purpose Input 1
FSITXA_D1	13			O	FSITX-A Data Output 1
GPIO102	0, 4, 8, 12	H3		I/O	General-Purpose Input Output 102
EMIF2_A4	3			O	External memory interface 2 address line 4
EQEP2_STROBE	5			I/O	eQEP-2 Strobe
SPIC_CLK	6			I/O	SPI-C Clock
ESC_GPI2	10			I	EtherCAT General-Purpose Input 2
FSITXA_CLK	13			O	FSITX-A Output Clock
GPIO103	0, 4, 8, 12	J1		I/O	General-Purpose Input Output 103
EMIF2_A5	3			O	External memory interface 2 address line 5
EQEP2_INDEX	5			I/O	eQEP-2 Index
SPIC_STEn	6			I/O	SPI-C Slave Transmit Enable (STE)
ESC_GPI3	10			I	EtherCAT General-Purpose Input 3
FSIRXA_D0	13			I	FSIRX-A Data Input 0
GPIO104	0, 4, 8, 12	J2		I/O	General-Purpose Input Output 104
I2CA_SDA	1			I/OD	I2C-A Open-Drain Bidirectional Data
EMIF2_A6	3			O	External memory interface 2 address line 6
EQEP3_A	5			I	eQEP-3 Input A
SCID_TX	6			O	SCI-D Transmit Data
ESC_GPI4	10			I	EtherCAT General-Purpose Input 4
CM-I2CA_SDA	11			I/OD	CM-I2C-A Open-Drain Bidirectional Data
FSIRXA_D1	13			I	FSIRX-A Data Input 1
GPIO105	0, 4, 8, 12	J3		I/O	General-Purpose Input Output 105
I2CA_SCL	1			I/OD	I2C-A Open-Drain Bidirectional Clock
EMIF2_A7	3			O	External memory interface 2 address line 7
EQEP3_B	5			I	eQEP-3 Input B
SCID_RX	6			I	SCI-D Receive Data
ESC_GPI5	10			I	EtherCAT General-Purpose Input 5
CM-I2CA_SCL	11			I/OD	CM-I2C-A Open-Drain Bidirectional Clock
FSIRXA_CLK	13			I	FSIRX-A Input Clock
ENET_MDIO_CLK	14			I/O	EMAC management data clock, Output in MII/RMII modes, Input in RevMII mode

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO106	0, 4, 8, 12			I/O	General-Purpose Input Output 106
EMIF2_A8	3			O	External memory interface 2 address line 8
EQEP3_STROBE	5			I/O	eQEP-3 Strobe
SCIC_TX	6	L2		O	SCI-C Transmit Data
ESC_GPI6	10			I	EtherCAT General-Purpose Input 6
FSITXB_D0	13			O	FSITX-B Data Output 0
ENET_MDIO_DATA	14			I/O	EMAC management data
GPIO107	0, 4, 8, 12			I/O	General-Purpose Input Output 107
EMIF2_A9	3			O	External memory interface 2 address line 9
EQEP3_INDEX	5			I/O	eQEP-3 Index
SCIC_RX	6	L3		I	SCI-C Receive Data
ESC_GPI7	10			I	EtherCAT General-Purpose Input 7
FSITXB_D1	13			O	FSITX-B Data Output 1
ENET_REVMII_MDIO_RST	14			I	EMAC REVMII MDIO reset
GPIO108	0, 4, 8, 12			I/O	General-Purpose Input Output 108
EMIF2_A10	3			O	External memory interface 2 address line 10
ESC_GPI8	10	L4		I	EtherCAT General-Purpose Input 8
FSITXB_CLK	13			O	FSITX-B Output Clock
ENET_MII_INTR	14			I/O	EMAC PHY interrupt, Input in MII/RMII mode, Output in RevMII mode
GPIO109	0, 4, 8, 12			I/O	General-Purpose Input Output 109
EMIF2_A11	3	N2		O	External memory interface 2 address line 11
ESC_GPI9	10			I	EtherCAT General-Purpose Input 9
ENET_MII_CRS	14			I	EMAC MII carrier sense
GPIO110	0, 4, 8, 12			I/O	General-Purpose Input Output 110
EMIF2_WAIT	3			I	External memory interface 2 Asynchronous SRAM WAIT
ESC_GPI10	10	M2		I	EtherCAT General-Purpose Input 10
FSIRXB_D0	13			I	FSIRX-B Data Input 0
ENET_MII_COL	14			I	EMAC MII collision detect
GPIO111	0, 4, 8, 12			I/O	General-Purpose Input Output 111
EMIF2_BA0	3			O	External memory interface 2 bank address 0
ESC_GPI11	10	M4		I	EtherCAT General-Purpose Input 11
FSIRXB_D1	13			I	FSIRX-B Data Input 1
ENET_MII_RX_CLK	14			I	EMAC MII receive clock
GPIO112	0, 4, 8, 12			I/O	General-Purpose Input Output 112
EMIF2_BA1	3			O	External memory interface 2 bank address 1
ESC_GPI12	10	M3		I	EtherCAT General-Purpose Input 12
FSIRXB_CLK	13			I	FSIRX-B Input Clock
ENET_MII_RX_DV	14			I	EMAC MII receive data valid (or) RMII carrier sense/ receive data valid
GPIO113	0, 4, 8, 12			I/O	General-Purpose Input Output 113
EMIF2_CAS	3	N4		O	External memory interface 2 column address strobe
ESC_GPI13	10			I	EtherCAT General-Purpose Input 13
ENET_MII_RX_ERR	14			I	EMAC MII / RMII receive error

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO114	0, 4, 8, 12	N3		I/O	General-Purpose Input Output 114
EMIF2_RAS	3			O	External memory interface 2 row address strobe
ESC_GPI14	10			I	EtherCAT General-Purpose Input 14
ENET_MII_RX_DATA0	14			I	EMAC MII / RMII receive data 0
GPIO115	0, 4, 8, 12	V12		I/O	General-Purpose Input Output 115
EMIF2_CS0n	3			O	External memory interface 2 chip select 0
OUTPUTXBAR5	5			O	Output X-BAR Output 5
ESC_GPI15	10			I	EtherCAT General-Purpose Input 15
FSIRXC_D0	13			I	FSIRX-C Data Input 0
ENET_MII_RX_DATA1	14			I	EMAC MII / RMII receive data 1
GPIO116	0, 4, 8, 12	W10		I/O	General-Purpose Input Output 116
EMIF2_CS2n	3			O	External memory interface 2 chip select 2
OUTPUTXBAR6	5			O	Output X-BAR Output 6
ESC_GPI16	10			I	EtherCAT General-Purpose Input 16
FSIRXC_D1	13			I	FSIRX-C Data Input 1
ENET_MII_RX_DATA2	14			I	EMAC MII receive data 2
GPIO117	0, 4, 8, 12	U12		I/O	General-Purpose Input Output 117
EMIF2_SDCKE	3			O	External memory interface 2 SDRAM clock enable
ESC_GPI17	10			I	EtherCAT General-Purpose Input 17
FSIRXC_CLK	13			I	FSIRX-C Input Clock
ENET_MII_RX_DATA3	14			I	EMAC MII receive data 3
GPIO118	0, 4, 8, 12	T12		I/O	General-Purpose Input Output 118
EMIF2_CLK	3			O	External memory interface 2 clock
ESC_GPI18	10			I	EtherCAT General-Purpose Input 18
FSIRXD_D0	13			I	FSIRX-D Data Input 0
ENET_MII_TX_EN	14			O	EMAC MII / RMII transmit enable
GPIO119	0, 4, 8, 12	T15		I/O	General-Purpose Input Output 119
EMIF2_RNW	3			O	External memory interface 2 read not write
ESC_GPI19	10			I	EtherCAT General-Purpose Input 19
FSIRXD_D1	13			I	FSIRX-D Data Input 1
ENET_MII_TX_ERR	14			O	EMAC MII transmit error
GPIO120	0, 4, 8, 12	U15		I/O	General-Purpose Input Output 120
EMIF2_WEn	3			O	External memory interface 2 write enable
ESC_GPI20	10			I	EtherCAT General-Purpose Input 20
FSIRXD_CLK	13			I	FSIRX-D Input Clock
ENET_MII_TX_CLK	14			I	EMAC MII transmit clock
GPIO121	0, 4, 8, 12	W16		I/O	General-Purpose Input Output 121
EMIF2_OEn	3			O	External memory interface 2 output enable
ESC_GPI21	10			I	EtherCAT General-Purpose Input 21
FSIRXE_D0	13			I	FSIRX-E Data Input 0
ENET_MII_TX_DATA0	14			O	EMAC MII / RMII transmit data 0

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO122	0, 4, 8, 12	T8		I/O	General-Purpose Input Output 122
EMIF2_D15	3			I/O	External memory interface 2 data line 15
SPIC_SIMO	6			I/O	SPI-C Slave In, Master Out (SIMO)
SD1_D1	7			I	SDFM-1 Channel 1 Data Input
ESC_GPI22	10			I	EtherCAT General-Purpose Input 22
ENET_MII_TX_DATA1	14			O	EMAC MII / RMII transmit data 1
GPIO123	0, 4, 8, 12	U8		I/O	General-Purpose Input Output 123
EMIF2_D14	3			I/O	External memory interface 2 data line 14
SPIC_SOMI	6			I/O	SPI-C Slave Out, Master In (SOMI)
SD1_C1	7			I	SDFM-1 Channel 1 Clock Input
ESC_GPI23	10			I	EtherCAT General-Purpose Input 23
ENET_MII_TX_DATA2	14			O	EMAC MII transmit data 2
GPIO124	0, 4, 8, 12	V8		I/O	General-Purpose Input Output 124
EMIF2_D13	3			I/O	External memory interface 2 data line 13
SPIC_CLK	6			I/O	SPI-C Clock
SD1_D2	7			I	SDFM-1 Channel 2 Data Input
ESC_GPI24	10			I	EtherCAT General-Purpose Input 24
ENET_MII_TX_DATA3	14			O	EMAC MII transmit data 3
GPIO125	0, 4, 8, 12	T9		I/O	General-Purpose Input Output 125
EMIF2_D12	3			I/O	External memory interface 2 data line 12
SPIC_STEn	6			I/O	SPI-C Slave Transmit Enable (STE)
SD1_C2	7			I	SDFM-1 Channel 2 Clock Input
ESC_GPI25	10			I	EtherCAT General-Purpose Input 25
FSIRXE_D1	13			I	FSIRX-E Data Input 1
ESC_LATCH0	14			I	EtherCAT LatchSignal Input 0
GPIO126	0, 4, 8, 12	U9		I/O	General-Purpose Input Output 126
EMIF2_D11	3			I/O	External memory interface 2 data line 11
SD1_D3	7			I	SDFM-1 Channel 3 Data Input
ESC_GPI26	10			I	EtherCAT General-Purpose Input 26
FSIRXE_CLK	13			I	FSIRX-E Input Clock
ESC_LATCH1	14			I	EtherCAT LatchSignal Input 1
GPIO127	0, 4, 8, 12	V9		I/O	General-Purpose Input Output 127
EMIF2_D10	3			I/O	External memory interface 2 data line 10
SD1_C3	7			I	SDFM-1 Channel 3 Clock Input
ESC_GPI27	10			I	EtherCAT General-Purpose Input 27
ESC_SYNC0	14			O	EtherCAT SyncSignal Output 0
GPIO128	0, 4, 8, 12	W9		I/O	General-Purpose Input Output 128
EMIF2_D9	3			I/O	External memory interface 2 data line 9
SD1_D4	7			I	SDFM-1 Channel 4 Data Input
ESC_GPI28	10			I	EtherCAT General-Purpose Input 28
ESC_SYNC1	14			O	EtherCAT SyncSignal Output 1
GPIO129	0, 4, 8, 12	T10		I/O	General-Purpose Input Output 129
EMIF2_D8	3			I/O	External memory interface 2 data line 8
SD1_C4	7			I	SDFM-1 Channel 4 Clock Input
ESC_GPI29	10			I	EtherCAT General-Purpose Input 29
ESC_TX1_ENA	14			I/O	EtherCAT MII Transmit-1 Enable

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO130	0, 4, 8, 12			I/O	General-Purpose Input Output 130
EMIF2_D7	3			I/O	External memory interface 2 data line 7
SD2_D1	7	U10		I	SDFM-2 Channel 1 Data Input
ESC_GPI30	10			I	EtherCAT General-Purpose Input 30
ESC_TX1_CLK	14			I	EtherCAT MII Transmit-1 Clock
GPIO131	0, 4, 8, 12			I/O	General-Purpose Input Output 131
EMIF2_D6	3			I/O	External memory interface 2 data line 6
SD2_C1	7	V10		I	SDFM-2 Channel 1 Clock Input
ESC_GPI31	10			I	EtherCAT General-Purpose Input 31
ESC_TX1_DATA0	14			O	EtherCAT MII Transmit-1 Data-0
GPIO132	0, 4, 8, 12			I/O	General-Purpose Input Output 132
EMIF2_D5	3			I/O	External memory interface 2 data line 5
SD2_D2	7	W18		I	SDFM-2 Channel 2 Data Input
ESC_GPO0	10			O	EtherCAT General-Purpose Output 0
ESC_TX1_DATA1	14			O	EtherCAT MII Transmit-1 Data-1
GPIO133	0, 4, 8, 12			I/O	General-Purpose Input Output 133
SD2_C2	7	G18	118	I	SDFM-2 Channel 2 Clock Input
AUXCLKIN	ALT			I	Auxilary Clock Input
GPIO134	0, 4, 8, 12			I/O	General-Purpose Input Output 134
EMIF2_D4	3			I/O	External memory interface 2 data line 4
SD2_D3	7	V18		I	SDFM-2 Channel 3 Data Input
ESC_GPO1	10			O	EtherCAT General-Purpose Output 1
ESC_TX1_DATA2	14			O	EtherCAT MII Transmit-1 Data-2
GPIO135	0, 4, 8, 12			I/O	General-Purpose Input Output 135
EMIF2_D3	3			I/O	External memory interface 2 data line 3
SCIA_TX	6	U18		O	SCI-A Transmit Data
SD2_C3	7			I	SDFM-2 Channel 3 Clock Input
ESC_GPO2	10			O	EtherCAT General-Purpose Output 2
ESC_TX1_DATA3	14			O	EtherCAT MII Transmit-1 Data-3
GPIO136	0, 4, 8, 12			I/O	General-Purpose Input Output 136
EMIF2_D2	3			I/O	External memory interface 2 data line 2
SCIA_RX	6	T17		I	SCI-A Receive Data
SD2_D4	7			I	SDFM-2 Channel 4 Data Input
ESC_GPO3	10			O	EtherCAT General-Purpose Output 3
ESC_RX1_DV	14			I	EtherCAT MII Receive-1 Data Valid
GPIO137	0, 4, 8, 12			I/O	General-Purpose Input Output 137
EPWM13A	1			O	ePWM-13 Output A (High-res available on ePWM1-8)
EMIF2_D1	3			I/O	External memory interface 2 data line 1
SCIB_TX	6	T18		O	SCI-B Transmit Data
SD2_C4	7			I	SDFM-2 Channel 4 Clock Input
ESC_GPO4	10			O	EtherCAT General-Purpose Output 4
ESC_RX1_CLK	14			I	EtherCAT MII Receive-1 Clock

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO138	0, 4, 8, 12	T19		I/O	General-Purpose Input Output 138
EPWM13B	1			O	ePWM-13 Output B (High-res available on ePWM1-8)
EMIF2_D0	3			I/O	External memory interface 2 data line 0
SCIB_RX	6			I	SCI-B Receive Data
ESC_GPO5	10			O	EtherCAT General-Purpose Output 5
ESC_RX1_ERR	14			I	EtherCAT MII Receive-1 Error
GPIO139	0, 4, 8, 12	N19		I/O	General-Purpose Input Output 139
EPWM14A	1			O	ePWM-14 Output A (High-res available on ePWM1-8)
SCIC_RX	6			I	SCI-C Receive Data
ESC_GPO6	10			O	EtherCAT General-Purpose Output 6
ESC_RX1_DATA0	14			I	EtherCAT MII Receive-1 Data-0
GPIO140	0, 4, 8, 12	M19		I/O	General-Purpose Input Output 140
EPWM14B	1			O	ePWM-14 Output B (High-res available on ePWM1-8)
SCIC_TX	6			O	SCI-C Transmit Data
ESC_GPO7	10			O	EtherCAT General-Purpose Output 7
ESC_RX1_DATA1	14			I	EtherCAT MII Receive-1 Data-1
GPIO141	0, 4, 8, 12	M18		I/O	General-Purpose Input Output 141
EPWM15A	1			O	ePWM-15 Output A (High-res available on ePWM1-8)
SCID_RX	6			I	SCI-D Receive Data
ESC_GPO8	10			O	EtherCAT General-Purpose Output 8
ESC_RX1_DATA2	14			I	EtherCAT MII Receive-1 Data-2
GPIO142	0, 4, 8, 12	L19		I/O	General-Purpose Input Output 142
EPWM15B	1			O	ePWM-15 Output B (High-res available on ePWM1-8)
SCID_TX	6			O	SCI-D Transmit Data
ESC_GPO9	10			O	EtherCAT General-Purpose Output 9
ESC_RX1_DATA3	14			I	EtherCAT MII Receive-1 Data-3
GPIO143	0, 4, 8, 12	F18		I/O	General-Purpose Input Output 143
EPWM16A	1			O	ePWM-16 Output A (High-res available on ePWM1-8)
ESC_GPO10	10			O	EtherCAT General-Purpose Output 10
ESC_LED_LINK0_ACTIVE	14			O	EtherCAT Link-0 Active
GPIO144	0, 4, 8, 12	F17		I/O	General-Purpose Input Output 144
EPWM16B	1			O	ePWM-16 Output B (High-res available on ePWM1-8)
ESC_GPO11	10			O	EtherCAT General-Purpose Output 11
ESC_LED_LINK1_ACTIVE	14			O	EtherCAT Link-1 Active
GPIO145	0, 4, 8, 12	E17		I/O	General-Purpose Input Output 145
EPWM1A	1			O	ePWM-1 Output A (High-res available on ePWM1-8)
ESC_GPO12	10			O	EtherCAT General-Purpose Output 12
ESC_LED_ERR	14			O	EtherCAT Error LED
GPIO146	0, 4, 8, 12	D18		I/O	General-Purpose Input Output 146
EPWM1B	1			O	ePWM-1 Output B (High-res available on ePWM1-8)
ESC_GPO13	10			O	EtherCAT General-Purpose Output 13
ESC_LED_RUN	14			O	EtherCAT Run LED
GPIO147	0, 4, 8, 12	D17		I/O	General-Purpose Input Output 147
EPWM2A	1			O	ePWM-2 Output A (High-res available on ePWM1-8)
ESC_GPO14	10			O	EtherCAT General-Purpose Output 14
ESC_LED_STATE_RUN	14			O	EtherCAT State Run

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO148	0, 4, 8, 12	D14		I/O	General-Purpose Input Output 148
EPWM2B	1			O	ePWM-2 Output B (High-res available on ePWM1-8)
ESC_GPO15	10			O	EtherCAT General-Purpose Output 15
ESC_PHY0_LINKSTATUS	14			I	EtherCAT PHY-0 Link Status
GPIO149	0, 4, 8, 12	A13		I/O	General-Purpose Input Output 149
EPWM3A	1			O	ePWM-3 Output A (High-res available on ePWM1-8)
ESC_GPO16	10			O	EtherCAT General-Purpose Output 16
ESC_PHY1_LINKSTATUS	14			I	EtherCAT PHY-1 Link Status
GPIO150	0, 4, 8, 12	B13		I/O	General-Purpose Input Output 150
EPWM3B	1			O	ePWM-3 Output B (High-res available on ePWM1-8)
ESC_GPO17	10			O	EtherCAT General-Purpose Output 17
ESC_I2C_SDA	14			I/OC	EtherCAT I2C Data
GPIO151	0, 4, 8, 12	C13		I/O	General-Purpose Input Output 151
EPWM4A	1			O	ePWM-4 Output A (High-res available on ePWM1-8)
ESC_GPO18	10			O	EtherCAT General-Purpose Output 18
ESC_I2C_SCL	14			I/OC	EtherCAT I2C Clock
GPIO152	0, 4, 8, 12	D13		I/O	General-Purpose Input Output 152
EPWM4B	1			O	ePWM-4 Output B (High-res available on ePWM1-8)
ESC_GPO19	10			O	EtherCAT General-Purpose Output 19
ESC_MDIO_CLK	14			O	EtherCAT MDIO Clock
GPIO153	0, 4, 8, 12	A12		I/O	General-Purpose Input Output 153
EPWM5A	1			O	ePWM-5 Output A (High-res available on ePWM1-8)
ESC_GPO20	10			O	EtherCAT General-Purpose Output 20
ESC_MDIO_DATA	14			I/O	EtherCAT MDIO Data
GPIO154	0, 4, 8, 12	B12		I/O	General-Purpose Input Output 154
EPWM5B	1			O	ePWM-5 Output B (High-res available on ePWM1-8)
ESC_GPO21	10			O	EtherCAT General-Purpose Output 21
ESC_PHY_CLK	14			O	EtherCAT PHY Clock
GPIO155	0, 4, 8, 12	C12		I/O	General-Purpose Input Output 155
EPWM6A	1			O	ePWM-6 Output A (High-res available on ePWM1-8)
ESC_GPO22	10			O	EtherCAT General-Purpose Output 22
ESC_PHY_RESETn	14			O	EtherCAT PHY Active Low Reset
GPIO156	0, 4, 8, 12	D12		I/O	General-Purpose Input Output 156
EPWM6B	1			O	ePWM-6 Output B (High-res available on ePWM1-8)
ESC_GPO23	10			O	EtherCAT General-Purpose Output 23
ESC_TX0_ENA	14			I/O	EtherCAT MII Transmit-0 Enable
GPIO157	0, 4, 8, 12	B10		I/O	General-Purpose Input Output 157
EPWM7A	1			O	ePWM-7 Output A (High-res available on ePWM1-8)
ESC_GPO24	10			O	EtherCAT General-Purpose Output 24
ESC_TX0_CLK	14			I	EtherCAT MII Transmit-0 Clock
GPIO158	0, 4, 8, 12	C10		I/O	General-Purpose Input Output 158
EPWM7B	1			O	ePWM-7 Output B (High-res available on ePWM1-8)
ESC_GPO25	10			O	EtherCAT General-Purpose Output 25
ESC_TX0_DATA0	14			O	EtherCAT MII Transmit-0 Data-0

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
GPIO159	0, 4, 8, 12	D10		I/O	General-Purpose Input Output 159
EPWM8A	1			O	ePWM-8 Output A (High-res available on ePWM1-8)
ESC_GPO26	10			O	EtherCAT General-Purpose Output 26
ESC_TX0_DATA1	14			O	EtherCAT MII Transmit-0 Data-1
GPIO160	0, 4, 8, 12	B9		I/O	General-Purpose Input Output 160
EPWM8B	1			O	ePWM-8 Output B (High-res available on ePWM1-8)
ESC_GPO27	10			O	EtherCAT General-Purpose Output 27
ESC_TX0_DATA2	14			O	EtherCAT MII Transmit-0 Data-2
GPIO161	0, 4, 8, 12	C9		I/O	General-Purpose Input Output 161
EPWM9A	1			O	ePWM-9 Output A (High-res available on ePWM1-8)
ESC_GPO28	10			O	EtherCAT General-Purpose Output 28
ESC_TX0_DATA3	14			O	EtherCAT MII Transmit-0 Data-3
GPIO162	0, 4, 8, 12	D9		I/O	General-Purpose Input Output 162
EPWM9B	1			O	ePWM-9 Output B (High-res available on ePWM1-8)
ESC_GPO29	10			O	EtherCAT General-Purpose Output 29
ESC_RX0_DV	14			I	EtherCAT MII Receive-0 Data Valid
GPIO163	0, 4, 8, 12	A8		I/O	General-Purpose Input Output 163
EPWM10A	1			O	ePWM-10 Output A (High-res available on ePWM1-8)
ESC_GPO30	10			O	EtherCAT General-Purpose Output 30
ESC_RX0_CLK	14			I	EtherCAT MII Receive-0 Clock
GPIO164	0, 4, 8, 12	B8		I/O	General-Purpose Input Output 164
EPWM10B	1			O	ePWM-10 Output B (High-res available on ePWM1-8)
ESC_GPO31	10			O	EtherCAT General-Purpose Output 31
ESC_RX0_ERR	14			I	EtherCAT MII Receive-0 Error
GPIO165	0, 4, 8, 12	C5		I/O	General-Purpose Input Output 165
EPWM11A	1			O	ePWM-11 Output A (High-res available on ePWM1-8)
MDXA	10			O	McBSP-A Transmit Serial Data
ESC_RX0_DATA0	14			I	EtherCAT MII Receive-0 Data-0
GPIO166	0, 4, 8, 12	D5		I/O	General-Purpose Input Output 166
EPWM11B	1			O	ePWM-11 Output B (High-res available on ePWM1-8)
MDRA	10			I	McBSP-A Receive Serial Data
ESC_RX0_DATA1	14			I	EtherCAT MII Receive-0 Data-1
GPIO167	0, 4, 8, 12	C4		I/O	General-Purpose Input Output 167
EPWM12A	1			O	ePWM-12 Output A (High-res available on ePWM1-8)
MCLKXA	10			O	McBSP-A Transmit Clock
ESC_RX0_DATA2	14			I	EtherCAT MII Receive-0 Data-2
GPIO168	0, 4, 8, 12	D4		I/O	General-Purpose Input Output 168
EPWM12B	1			O	ePWM-12 Output B (High-res available on ePWM1-8)
MFSXA	10			O	McBSP-A Transmit Frame Sync
ESC_RX0_DATA3	14			I	EtherCAT MII Receive-0 Data-3
TEST, JTAG, AND RESET					
ERRORSTS		U19	92	O	Error Status Output. When used, this signal requires an external pulldown.
FLT1		W12	73	I/O	Flash test pin 1. Reserved for TI. Must be left unconnected.

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
FLT2		V13	74	I/O	Flash test pin 2. Reserved for TI. Must be left unconnected.
NC		H4	119		No Connection. This pin is not internally connected to the device. This pin may be left open or connected to any voltage within the maximum operating conditions.
TCK		V15	81	I	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK.
TDI		W13	77	I	JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO		W15	78	O	JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK.
TMS		W14	80	I	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. An external pullup resistor (recommended 2.2 kΩ) on the TMS pin to VDDIO should be placed on the board to keep JTAG in reset during normal operation.
TRSTn		V14	79	I	JTAG test reset with internal pulldown. TRSTn, when driven high, gives the scan system control of the operations of the device. If this signal is driven low, the device operates in its functional mode, and the test reset signals are ignored. NOTE: TRST must be maintained low at all times during normal device operation. An external pulldown resistor is required on this pin. The value of this resistor should be based on drive strength of the debugger pods applicable to the design. A 2.2-kΩ or smaller resistor generally offers adequate protection. The value of the resistor is application-specific. TI recommends that each target board be validated for proper operation of the debugger and the application. This pin has an internal 50-ns (nominal) glitch filter.
X1		G19	123	I	Crystal oscillator input or single-ended clock input. The device initialization software must configure this pin before the crystal oscillator is enabled. To use this oscillator, a quartz crystal circuit must be connected to X1 and X2. This pin can also be used to feed a single-ended 3.3-V level clock.
X2		J19	121	O	Crystal oscillator output.
XRSn		F19	124	I/OD	Device Reset (in) and Watchdog Reset (out). During a power-on condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the XRSn pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor between 2.2 kΩ and 10 kΩ should be placed between XRSn and VDDIO. If a capacitor is placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to VOL within 512 OSCCLK cycles when the watchdog reset is asserted. The output buffer of this pin is an open-drain with an internal pullup. If this pin is driven by an external device, it should be done using an open-drain device. If this pin is driven by an external device, it should be done using an open-drain device.

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
POWER AND GROUND					
VDD		E9, E11, F9, F11, G14, G15, J14, J15, K5, K6, P10, P13, R10, R13	61, 76, 117, 126, 137, 153, 158, 169, 16, 21		1.2-V Digital Logic Power Pins. TI recommends placing a decoupling capacitor near each VDD pin with a minimum total capacitance of approximately 20 µF. The exact value of the decoupling capacitance should be determined by your system voltage regulation solution. A single 56Ω resistor (10% tolerance) should be placed between between VDD and VSS. This resistor provides a load to consume an internal VDD3VFL to VDD current source and avoid VDD voltage rising during low power device conditions.
VDD3VFL		R11, R12	72		3.3-V Flash power pin. Place a minimum 0.1-µF decoupling capacitor on each pin
VDDA		P6, R6	54, 36		3.3-V Analog Power Pins. Place a minimum 2.2-µF decoupling capacitor to VSSA on each pin.
VDDIO		A9, A18, B1, E7, E10, E13, F7, F10, F13, G5, G6, H5, H6, L14, L15, M1, M5, M6, N14, N15, P9, R9, V19, W8, F4, G4, E16, F16	62, 68, 75, 82, 88, 91, 99, 106, 114, 116, 127, 138, 147, 152, 159, 168, 3, 11, 15, 20, 26		3.3-V Digital I/O Power Pins. Place a minimum 0.1-µF decoupling capacitor on each pin.
VDDOSC		H16, H17	120, 125		Power pins for the 3.3-V on-chip crystal oscillator (X1 and X2) and the two zero-pin internal oscillators (INTOSC). Place a 0.1-µF (minimum) decoupling capacitor on each pin.

Table 6-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	337	176	PIN TYPE	DESCRIPTION
VSS		A1, A10, A19, E5, E6, E8, E12, E14, E15, F5, F6, F8, F12, F14, F15, G16, G17, H8, H9, H10, H11, H12, H14, H15, J5, J6, J8, J9, J10, J11, J12, K8, K9, K10, K11, K12, K14, K15, L5, L6, L8, L9, L10, L11, L12, L18, M8, M9, M10, M11, M12, M14, M15, N1, N5, N6, P7, P8, P11, P12, P14, P15, R7, R8, R14, R15, W7, W19	178, 179, 180, 177		Digital Ground
VSSA		P1, P5, R5, V7, W1	52, 34		Analog Ground
VSSOSC		H18, H19	122		Crystal oscillator (X1 and X2) ground pin. When using an external crystal, do not connect this pin to the board ground. Instead, connect it to the ground reference of the external crystal oscillator circuit. If an external crystal is not used, this pin may be connected to the board ground.